Real-Time Simulation of VSC-based HVDC Systems using Rectification Capable Switching Function-Based 3-Level Inverter Models

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Abstract- This paper presents a simulation model of a 3-level Neutral-Point Clamped IGBT inverter bridge suitable for real-time simulation testing. The model is switching-function based but also works in rectifying mode. Because of the large number of individual switches that compose such an inverter, the switching-function approach produces exceptional computational speed gain when compared to piecewise time-segment linear algorithms such as SimPowerSystems, both in off-line and real-time modes. A benchmark comparison of the model used in an HVDC-VSC application with the RT-LAB simulator has shown a 10-fold increase in hard real-time computational speed.

I. INTRODUCTION

Traditional HVDC transmission systems are based on current source converters with line-commutated thyristor switches. In recent years, with advances in design of high power sled-commutated devices like GTOs and IGBTs, a new configuration of HVDC systems has emerged: Voltage-Source-Converter HVDC systems (VSC-HVDC)[1]. The VSC-HVDC topology brings new possibilities in the design of a power system. They can feed very weak AC systems and can provide independent active and reactive control with a very fast time response. However, they still present a higher cost on a per kW basis.

The emergence of the VSC-HVDC technology has simultaneously raised the requirements for tests of the devices. The financial and economic risks associated with this new technological trend impose serious requirements for power system designers. A typical method to test such equipments is to use real-time simulators. First, the controllers of VSC-HVDC systems can be tested against a real-time simulated equivalent of the VSC-HVDC system. This is called Hardware-In-the-Loop (HIL) simulation. In this set-up, the real (controllers) and simulated (power system) parts of the complete apparatus only exchange low-power sensors and IGBT gate signals. Real-Time Simulator laboratories for electrical system HIL testing are used in the automotive industry[2][3], companies involved in drive design[3][4][5] utilities[6][7][8] and for university research[9][10][11].

Whenever possible, power system designers go even further in pre-deployment tests by testing the actual power device and associated controllers against a simulated grid. In this situation, the power device under test (DUT) must have real power exchange with the simulated grid. This is achieved by driving the DUT with power amplifiers controlled by the simulation values. This real-time test configuration is sometimes called Power-HIL.

The real-time simulation of large power systems is difficult for several reasons. The main reason is the size of the network that can be simulated in a specified amount of time with the available computational engine available. A less obvious difficulty resides in the large number of switches that a system contains. Typical power system solvers based on binary modeling of switches need to recalculate equations each time a switch conduction state changes. In a real-time simulation paradigm, when a large number of switches are present in the simulated systems, this results in different problems that depend on the simulation approach. In the nodal approach, maximum retriangularisation time increases with the number of switches. In SimPowerSystems (SPS), the matrix equation update routine also gets longer with the increase in the number of switches. With SPS and the ARTEMIS real-time plug-in[12][13], the memory requirements for the storage of a discrete state-space matrix for all possible switch position combinations may exceed the actual memory that is available on the simulator.

Switching function based inverter models can alleviate these problems because they do not include the switch in the main system equations. Instead, they mimic switch actions by ‘routing’ voltage and currents across the components to which they are connected. For example, the middle point of an IGBT inverter leg will be either connected to the V+ bus or the ground, as a function of the IGBT gate levels. Anti-parallel diode action can also be taken into account this way. This type of model usually assumes the condition of constant conduction of the load. When the condition is not fulfilled, the model doesn’t work[14]. This is the case when, for example, an IGBT inverter is used in rectifying mode with all IGBT pulses disabled.

II. SWITCHING-FUNCTION BASED 3-LEVEL INVERTER WITH RECTIFYING CAPABILITIES

The 3-level inverter is based on previously published work. In addition to the regular working mode, where interpolation of the terminal voltage is made in real-time, the block also implements some logic that makes it work in rectifying mode.
For this purpose, the bridge needs a BackEMF voltage so it can determine the proper anti-parallel diode turn-on event in the free-running mode (where all IGBT pulses are OFF and the load current is zero at some time). If this line-to-line BackEMF voltage is greater than the DC-link voltage, some diodes turn ON.

In contrast to the active control mode, the free-running mode exhibits some high-impedance state on the part of the inverter. The problem is that the inverter itself is switching function based and therefore cannot mimic a high impedance state. Therefore, the inverter needs to be able to set its load in high impedance. In the SPS model, this is accomplished by inserting breakers between the inverter and its load. The inverter can then control its overall impedance state by acting on the breakers.

This model has the disadvantage of explicitly demanding the BackEMF signal and therefore requires modification of the system model to provide this value. Some SimPowerSystems coding would be required to obtain this BackEMF value without modification to the Simulink graphical interface.

III. VSC-BASED HVDC SYSTEM DEMO

The proposed 3-level inverter has been tested on a VSC-Based HVDC system. The tested model is taken from SimPowerSystems demo power_hvdc_vsc.mdl[15]. It consists of a 200 MVA (+/- 100 kV DC) forced-commutated Voltage-Sourced Converter (VSC) interconnection used to transmit power from a 230 kV, 2000 MVA, 50 Hz system to another identical AC system. The rectifier and the inverter are three-level Neutral Point Clamped (NPC) VSC converters using IGBT/Diodes. The PWM frequency of the inverters is set equal to 27 times the fundamental frequency (1350 Hz). The stations also have 40 MVAR shunt AC filters (27th and 54th high-pass) tuned around the two dominating harmonics. The DC links have high-frequency blocking filters tuned to the 3rd harmonic, i.e. the main harmonic present in the positive and negative pole voltages.

The rectifier and the inverter are interconnected through a 75 km cable and two 8 mH smoothing reactors. A circuit breaker is used to apply a three-phase to ground fault on the inverter AC side. Also, for testing purposes, voltage sags can be applied to the Station 1 side.

The inverter and rectifier parts are controlled in different ways. The inverter part is in charge of regulating the DC-link voltage as well as the reactive power of its station. The rectifier part controls the actual DC power flow (or the current flow since the voltage regulation is made by the inverter) as well as the reactive power. The fact that we deal with voltage inverters almost automatically means that we can regulate reactive power because the inverter voltage amplitude is simply controlled by the applied modulation index.
IV. ACCURACY OF THE PROPOSED MODEL IN HVDC-VSC

The proposed model accuracy has been compared with the regular SimPowerSystems model in a typical simulation scenario involving a VSC-HVDC system. A comparison of the two simulations is shown in Fig. 3, where the SimPowerSystems results are on the left side and the proposed model results are on the right side. The test scenario goes through the following stages:

- Upon system start-up, all controls are disabled and the DC-link charges through anti-parallel diodes of the inverters.
- At 0.1 sec., the inverter-side station begins to regulate the DC-link voltage.
- Then at 0.3 sec., the rectifier station begins to regulate the DC power on the link.
- Then, at 1.5 sec, the rectifier-side AC source amplitude is dropped by 0.1 pu for 0.14 sec.
- A 6-cycle 3-phase fault is then applied at 2.1 sec.

The simulation results for the above test scenario are shown in Fig. 3. The regular SimPowerSystems simulation (left) is very similar to the one where the 3-level inverter has been replaced with a switching-function-based inverter.

An important part of the simulation is the pre-charge stage where the DC-link gets charged by natural rectifications on the inverter diodes. This happens in the beginning of the simulation and the proposed inverter model shows the same accuracy as the SPS model.

V. REAL-TIME PERFORMANCE OF THE HVDC-VSC MODEL

The proposed 3-level inverter model calculation speed has been evaluated in RT-LAB with the complete model along with its controls in one unique CPU. The maximum calculation time obtained is shown in TABLE 1.

| TABLE 1. MAXIMUM CALCULATION TIME FOR MODEL POWER_HVDC_VSC (DUAL-CORE PENTIUM 2.2 GHZ) |
|-----------------------------------|-----------------|
| Model with Proposed 3-level inverter | 44 µs |
| Regular SimPowerSystems model | 380 µs |

The VSC-HVDC system computational time is about 10 times faster with the proposed 3-level inverter than with regular 3-level inverter model from SimPowerSystems. The relatively long computational time of SPS is mainly caused by the treatment of switches by SPS solvers.
TABLE 1 timings are for the simulation of the complete VSC-HVDC and controllers on a single CPU. Since the HVDC stations are separated by 75 km lines, it would be possible to simulate each station on a separate CPU (with the decoupling property of line propagation delay) and cut this timing by half.

It is also important to note that the timing refers to the maximum execution time of all time steps (critical in HIL applications) and not the average calculation time (more important in standard simulation).

VI. ADDITIONAL TESTS

In this section, we will test the proposed inverter model on a 2nd power system, a simple AC/DC three-level PWM converter, depicted in Fig. 4. The model, power_3levelSVC.mdl, is again taken from the SimPowerSystems demos[16]. It is composed of a 3-phase inductive source (600V) connected on the AC-side to a 500 kVar capacitor bank and 1 MW load. A 400kW DC-load is fed by a three-level inverter connected on this AC-bus through a transformer and a reactor. The controller tries to regulate the DC voltage to 500V despite load variations (200kW added at T=0.05 sec. form the initial 200kW). Then, at T=0.1 sec, the IGBT pulse are blocked and the inverter goes into rectifying mode. Fig. 5 compares the DC link voltages and transformer input currents between an SPS model running at 5 us and the proposed model (TSB) at 25 us, this last sample time being compatible with current real-time CPU-based simulator technology. They are very similar both in active mode and in rectifying mode (after 0.1 sec.).

Not shown in the result tests is the rectifying to active mode transition. At the time of writing this paper, this transition results in some DC-link over-voltage for this circuit (>20% with regards to the SimPowerSystems reference). The authors are actively working to further improve the model. It must be mentioned that the major usage of the real-time simulator for the inverter-based controller development is made in the active mode.

![AC/DC Three-Level PWM Converter](image)

**AC/DC Three-Level PWM Converter**

![Grid-connected 3-level PWM converter (power_3levelSVC.mdl)](image)

**Fig. 4** Grid-connected 3-level PWM converter (power_3levelSVC.mdl)

![DC-link voltage (left) and Transformer input current (right): comparison between SPS and proposed inverter model (TSB)](image)

**Fig. 5** DC-link voltage (left) and Transformer input current (right): comparison between SPS and proposed inverter model (TSB)
CONCLUSION

This paper has presented a real-time model of a 3-level Neutral-Point Clamped IGBT inverter. The model is suitable for Hardware-In-the-Loop testing of VSC-Based HVDC controllers and has a hard real-time time step below 50 us on the RT-LAB real-time simulation platform.

A further increase in computational speed is possible by the use of the latest generation of CPUs from Intel or AMD. Further increase in speed can also be obtained by distributing the tasks of the model on several CPUs. This is in fact quite possible because the HVDC stations are separated by relatively long transmission lines and also that the VSC-HVDC controllers could be simulated either on a separate CPU or even not at all in the case where the controllers are external devices to the simulator (HIL simulation).

The paper also shows that the proposed model achieves a very high degree of accuracy when compared to regular SimPowerSystems models. This has been shown in the paper by comparing the inverter model response for a complete VSC-HVDC link, for steady state and faulty modes.

REFERENCES