Hardware-In-the-Loop Simulation of Power Drives with RT-LAB

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Abstract -- This paper presents the RT-LAB Electrical Drive Simulator technology along with practical applications. The RT-LAB simulation software enables the parallel simulation of power drives and electric circuits on clusters of PC running QNX or RT-Linux operating systems at sample time below 10 μs. Using standard Simulink models including SimPowerSystems models, RT-LAB build computation and communication tasks necessary to make parallel simulation of electrical systems with standard off-the-shelf PCs and communication links like InfiniBand. To accommodate the high bandwidth of electrical systems, the RT-LAB Electrical Drive Simulator comes with special Simulink-based modeling tools, namely ARTEMIS and RT-Events that permits real-time simulation of electrical systems at practical time step of 10 μs but with sub-μs equivalent precision through the use of interpolation techniques. For power drives with even higher bandwidth, RT-LAB XSG permits simulation of PMSM drive at 1 μs on FPGA with VHDL code generated from Xilinx System Generator.

Keyword - Hardware-in-the-loop simulation, Motor Drives, Power Electronics, Real-Time Simulation, FPGA simulation

I. INTRODUCTION

Automatic code generation software such as Real-Time Workshop and Autocode has made it possible to build very powerful real-time simulators like RT-LAB without writing any code by hand. An engineer can now go directly from a Simulink or SystemBuild simulation to hardware implementation with minimal debugging time. Since the introduction of real-time simulation, two major applications have emerged: rapid prototyping of controllers and Hardware-in-the-Loop (HIL) testing of production-line controllers. In rapid prototyping, a controller is first modeled in Simulink and the model is then compiled to run on a specified target system allowing testing of the controller algorithm against a real plant. In HIL simulation testing of production-line controllers, the actual controller is tested against a simulated plant model running in the real-time simulator.

While controller rapid-prototyping is a well-established technique, the HIL plant simulation technique is more difficult to realize for electrical systems for several reasons. For example, electrical systems usually have a lot of working modes caused by switches. Electrical systems also tend to be “stiff” by nature, requiring very small time steps or variable-step solvers to achieve convergence and/or accuracy.

The last difficulty comes from the use of power electronic switching devices running at high commutation frequencies. Emulating an IGBT motor inverter requires sub-microsecond precision on the firing time. This is problematic in HIL simulation where current hardware can barely simulate the system at a 10 μs time step. For power network simulation, even such a small time step requires special solvers and interpolation techniques to ensure accurate results.

This paper introduces the RT-LAB Electric Engineering simulator. The paper describes the hardware and software solutions used with some example applications for HIL simulation of electrical systems and drives. The paper put special emphasis on solution technique to accurately simulate high-frequency PWM drive and converters.

II. THE RT-LAB REAL-TIME SIMULATOR

The RT-LAB simulator is designed to make the real-time simulation of Simulink or SystemBuild models on clusters of standard Pentium-based multi-CPU PCs.

RT-LAB runs real-time simulation of Simulink model on multi-CPU computer with shared memory. PC-based systems with dual-core processor like the dual-core Opteron (single or dual version) or Dual-Pentium processors are commercially available for this purpose. RT-LAB build parallel tasks from the original Simulink model and run them on each CPU of the multi-CPU computer. Data are exchanged though shared-memory that has ultra-low latency in the same order of the CPU system memory and thus permits the parallel simulation of electrical systems at time step below 10 μs.
For larger systems, RT-LAB can also make real-time distributed simulation across a cluster of PCs. This involves transmitting data between CPUs on separate PC through external communication links. To achieve this, RT-LAB can use an FPGA-based proprietary communication link called SignalWire™ capable to deliver up to 1.25 Gbit/s transfer rates, with a latency of 200 ns or an InfiniBand switch.

The same FPGA board implements useful functionalities for hardware-in-the-loop testing of electrical systems. The RT-LAB platform is configured to be used with a supplied library of Simulink blocks that allow the user to implement the DIO, event capture, event generation, and PWM I/O capabilities, all with 10 ns resolution, in the real-time model without coding.

The RT-LAB simulator also support for most commercially available I/O cards like Sensoray, NI and Acromag. It can also by easily interfaced with automated test software like TestStand from NI and various simulation tools like like CarSim, LabView and Altia for example.

A. RT-LAB XSG

The kind of FPGA task mapping made with basic I/O functions is only the first step toward Sim-On-Chip technology in which more general simulation tasks, for example a motor drive, are mapped to the FPGA core. With RT-LAB XSG, the motor drive is graphically programmed and tested using Xilinx System Generator (XSG). XSG then automatically generates VHDL code and bitstreams for direct FPGA execution.

In hardware-in-the-loop applications, this technology will permit to avoid the latency time of the PCI bus of standard PC by grouping model and I/O and simulation time step below 1 μs are expected. This speed will be sufficient to test controller with sampling loop below 10 μs.

III. ARTEMIS: DEALING WITH SWITCHED POWER NETWORKS IN REAL TIME

The ARTEMIS software is a blockset from Opal-RT Technologies for the SimPowerSystems (SPS) blockset for Simulink. It permits real-time simulation of SPS schematics under Real-Time Workshop and RT-LAB software. ARTEMIS improves the real-time simulation capability of standard Simulink SimPowerSystems schematics with the following characteristics:

- High precision discretisation methods in addition to the SPS trapezoidal rule of integration
- Equation parallelization of network containing distributed parameter lines or other decoupling devices.
- Cached precalculation of network equations for some or all switch position topologies (circuit modes).
- Interpolation for switching events occurring between time steps.

Precomputation of circuit modes due to switch position is critical to obtain real-time simulation performance from SimPowerSystems because it removes the mode equation calculation (i.e. finding the content of the A, B, C, D matrix) from the real-time loop leaving only the iteration part (multiply-addition of A, B, C, D matrix with inputs and state vectors) in this loop.

Interpolation capability is an important feature in real-time simulation to keep acceptable accuracy despite the computational time constraint of real-time simulation. ARTEMIS interpolation algorithm[1] is especially designed to deal with this limitation by avoiding double interpolation scheme used in all other real-time simulation platforms.

IV. TIME STAMPED BRIDGES: PRECISE SIMULATION OF HIGH-FREQUENCY PWM INVERTERS AND DC-DC CONVERTERS

The problem of electrical system simulation can get bad when simulating power converters like PWM motor inverters and DC-DC converters because of their high switching frequencies with regards to the simulation sampling frequency, i.e. the inverse of the time step. One of those problem concerns the accurate time sampling of IGBT gate signals. In AC motor drives for example, accurate motor flux integration is dependant upon the precise sampling of the IGBT gate signals by the simulator. This sampling must have sub-μs precision while typical real-time simulation time step are in the 10-50 μs range. There are solutions to this problem.

a) In fully numerical real-time simulation where controllers and plant are simulated, the IGBT gate signals generation must be made with equivalent sub-μs resolution despite the fixed-time simulation. This requires the use of RT-Events, a Simulink blockset designed for interpolation of in-step events in models like the sinus-triangular comparisons occurring in PWM generation.

b) In real-time HIL simulation where the simulated motor inverter is interacting with an external controller, the IGBT gate signals must be sampled by high frequency counter cards (like Opal-RT FPGA card) and the resulting time stamp incorporated into the simulation process by some interpolation technique.

In both cases, the IGBT bridge model must be able to use this interpolation information to compensate the simulation process. Time Stamped Bridge models do just that.

Take for example the simple chopper drive of Figure 1 where the load current should be linearly dependant upon the chopper duty-cycle. It happens that the simulation of this drive at 10 μs time step and a 10 kHz choppin frequency (resulting in a sampling to PWM frequency ratio of 10) leads to gross inaccuracies when the simulation is uncompensated like in SimPowerSystems blockset with discrete simulation option (Figure 2, curve r).
In contrast, compensated fixed step simulation tools like the RT-Events blockset from Opal-RT Technologies lead to accurate simulation (Figure 2, curve b). This works because RT-Events blocks propagate zero crossing information at fixed time step and the Time Stamped Bridge use this information to produce compensated output voltages to the load.

These TSB models can even accurately simulate dead time effect lower that the simulation fixed time step! Figure 3 shows the steady-state current level drop at the load when increasing the IGBT leg dead time. In this figure, the TSB simulates perfectly 4.9 A per μs of dead time current drop computed from theory.

The Time Stamped Bridge models of the RT-Events blockset are an effective method to simulate power inverters. The technique is accurate on inverters working in continuous conduction mode. It must by noted that ARTEMIS could also deal with the same inverter with equivalent accuracy because of its interpolating capability. The Time Stamped Bridge is much faster though because it does not involve the state space formulation of network equations used in ARTEMIS and SimPowerSystems.

V. EXAMPLE OF REAL TIME SIMULATION OF MOTOR DRIVE AND OTHER ELECTRIC DEVICES

This section will show some actual real time simulation of motor drives and power converters. Those examples are a PMSM drive with AC-side diode rectifier, fuel cell hybrid vehicle drive and converters, train traction drive (3-level GTO inverter PMSM drive with 12-pulse thyristor rectifier) and 9-level inverter drive with 3-phase 13-winding feeding transformer.

A. PMSM drive with AC-side diode rectifier

The circuit of Figure 4 represents a permanent magnet synchronous motor (PMSM) drive fed by a 3-phase diode rectifier. The diode rectifier uses the ARTEMIS blockset to precompute all modes of the rectifier, thus removing SimPowerSystems mode computation from the real-time loop. A TSB is used to model the IGBT bridge so to accurately compute the voltage-time application time to the motor model (which itself integrates this voltage into fluxes). This is important because if the model where to sample the IGBT gate signals at 10 μs without special care, important error would occur in the motor fluxes computation with the PWM carrier set at 9 kHz (about 14 times the 125 kHz sampling frequency of the simulator).
A real-time simulator running this model has been successfully commissioned by Opal-RT for Mitsubishi Electric Co. of Japan in August 2004 [7]. The model is connected to a real external vector controller with a sampling rate of 55 μs. The external controller reads the motor currents and the quadrature encoder signals from the simulator and feeds the simulator with the 6 IGBT gate signals. The complete model runs, in HIL mode on 3.6 GHz dual-Xeon PCs, at a sample time of 8 μs for the CPU simulating the inverter and 64 μs for the CPU running the AC-side of the model.

In Figure 6 the dead time of the inverter was modified and its effect on motor current studied. An increase in dead time increases the safety of the design but results in higher distortion of the currents. Benefits of use of a real-time simulator extend beyond classic testing of production-class controller and into the design and optimisation process. The fidelity of simulation of TSB, AC-link and PMSM models enables designers to accelerate optimisation through batch run test that use the real-time simulator in off-line mode. This off-line mode can be even more rapid than the HIL mode and results in significant time savings. For example, 10 seconds simulation of the PMSm drive of Figure 4 sometimes take 7 hours in Simplorer while it simulates in real-time with the RT-LAB simulator.

B. Fuel Cell Hybrid Electric Vehicle Drive

The circuit of Figure 7 represents a fuel cell hybrid electric vehicle (FCHV) drive system composed of a battery, a fuel cell, a DC-DC converter and motor drive [3][4]. The fuel cell model can be either very simple like V-I curve emulation or include detailed chemical and thermal effects[5].

In the FCHV topology of Figure 7 the role of the DC-DC converter is to control the power flow at the battery. In steady state, one wants the power to come uniquely from the fuel cell while the battery can absorb and restitute power during transients like acceleration and braking of the traction motor.

Figure 8 shows the simulation results for the FCHV as outputted by the RT-Scope interface of RT-LAB, an alternative to Simulink scopes. In the test, a square wave speed perturbation is applied on the PMSM. One can see the slow time response of the fuel cell (bottom scope, upper curve) and the fast response of the of the battery power (bottom scope, lower trace).

Figure 5 and Figure 6 shows the HIL simulation results, captured on a real oscilloscope, of the PMSM drive. On the first figure, the PWM carrier was modified for a constant dead time of 4.2 μs. As expected, the current ripple diminished when the PWM frequency is augmented. This current ripple causes electrical torque ripples that can affect overall system performances.
reached, the motor currents drop again. At this stage, the battery supplies the traction motor with power because fuel cell power is still 0 and rising slowly. One can notice that during deceleration, the battery power is less negative than motor power, the difference causing DC-link to charge. When the motor comes to constant low speed, the DC-link voltage is to high for the fuel to produce a lot of power.

It is worth noticing that the actual usage of this interface results in stable visualization because the acquisition is triggered on the perturbation signal (PMSM speed rise front edge). This kind of user interface is also very useful to modify signals type of model parameters like motor speed, torque, dead time and perturbation parameters (right part of the GUI).

This testing process can also be automated by using batch testing software like TestStand from National Instruments. RT-LAB API permits easy interfacing with this kind of automated test software package.

C. Train Traction Drive

The train traction drive described in Figure 9 is composed of a grid-connected 12-pulse thyristor rectifier connected to a 3-level GTO inverter feeding a 1 MW permanent magnet motor.

The 3-level GTO inverter is modeled with Time Stamped Bridge and ARTEMIS was used to achieve hard real-time simulation of the AC-side rectifier. Furthermore, a special transformer model from the Real-Time Models library from Opal-RT is used to artificially decouple the two secondary windings of the transformer so that full precomputation of the two 6-pulse thyristor modes could be made by ARTEMIS. If this is not done then the algorithm have to precompute $2^{12} = 4096$ different system equations for the AC-side only.

The principle used to introduce the decoupling at the secondary windings is to model the secondary leakage inductance by a short transmission line (sometimes called a “stubline”) having the same line inductance. The approximation has then the effect of introducing some line capacitances that are not really present in the circuit. As long as the sample time is small, the spurious capacitances are also small and the error is minimal.

The model is simulated on a dual-CPU PC and takes advantage of the fact that the voltage of the DC-link capacitors do not change much during a single time step. Therefore, introducing a one step delay in DC-link voltage and bridge current values transmission between CPUs causes minimal errors.

This complete drive with Simulink controllers runs at sample time of 19 $\mu$s on a 2.4 GHz Dual Xeon PC running RT-LAB with RedHawk Linux real-time operating system.
D. Nine-level inverter with 13-winding three-phase transformer

The multi-level inverter shown in Figure 11 is a high-power ultra-low harmonic generating inverter drive. By feeding the DC-stage from winding with different phases, the injected harmonics are minimized at the primary. Nine-level inverter also provides low harmonics at the load. Time Stamped Bridges are used to model the inverter circuit while the use of a special decoupling transformer (again stubline-based) in conjunction with ARTEMIS permits full mode precomputation of this model and achieve real-time simulation under 60 μs time step (30 us for the CPU with the inverter part) on a dual Xeon 3.6 GHz computer.

Figure 11 Nine-level inverter with 13-winding feeding transformer

Figure 12 shows the resulting voltage at the load. Simulating 48 switches with regular SimPower Systems models may takes more than 300 μs like in a 48-pulse STATCOM models[8]. The TSB models are 10 times more rapid in this case.

![Figure 12](image)

**Figure 12** Load voltage for the nine-level inverter

VI. Conclusion

This paper has presented the RT-LAB simulator along with some typical example of real-time simulation of power drives and converters. IGBT converters were simulated with Time Stamped Bridges while line commutated rectifiers used ARTEMIS and SimPowerSystems. In the cases where the line rectifiers had too many modes for complete pre-computation of modes, special stubline-based transformer models where used to achieve real-time performance.

Usage of interpolation techniques is demonstrated to be very important with the 3-level inverter of the train traction drive. Interpolation is also demonstrated to be very important for the FCHV case (see [3][5]) and the PMSM drive with AC-diode rectifier [7] as well as in other PWM drive application like large induction motor drive simulation[6], wind-turbine application[2] and even for matrix converters[9].

Time Stamped Bridges are an excellent alternative to average models because they interface naturally with the IGBT signals, both in HIL and fully numerical modes of simulation. They are accurate for Sampling-to-PWM frequency ratio greater than 10 and slowly become equivalent to average models below that ratio.

**References**


