All Products Release Notes

Communication Protocols | eFPGASIM | eMEGASIM | ePHASORSIM | RT-LAB | RT-XSG

Latest Update: October 11, 2018

CONTENTS

Version 11.3.3

Features

- ePHASORsim: New environment variables to do network/data validations and get more logs and verbose output (EP-1382 and EP-1385).

- ePHASORsim: FMU interface now needs platform individual based FMUs, instead of one file that includes both. All the FMU built in previous versions must be regenerated with FMUCreator in this version (EP-1372).

- MIL-STD-1553: Added support of QPCX-1553 4 channels card (DRV-2701).

- OP4200: Added option to enable/disable automatic bitstream reprogramming (DRV-2777).

- DINAMO: Added new example model.

Bugfixes

- RT-LAB: Fixed application of PARAM_VECTOR_SIZE_LIMIT variable. Very useful for DINAMO (RTLABTT-1216).

- RT-LAB: Fixed projects that were not closing when variable table contains signal and is opened (RTLABTT-1214).

- RT-LAB: Fixed "ConfigModifiedPinger: java null pointer" that may appears sometimes (RTLABTT-1251).

- RT-LAB: Fixed many problems related to variables table refresh (RTLABTT-1241, RTLABTT-2241, RTLABTT-1226).

- RT-LAB: Fixed matlab variable support: remove support for vectors and structures (RTLABTT-1220).

- DINAMO: Fixed many problems and crash when using PEST (RTLABTT-1242, RTLABTT-1243, RTLABTT-1244, RTLABTT-1246, RTLABTT-1247).

- Synchronization: Fixed advanced parameters when synchronized by IRIG-B or 1PPS (DRVTT-555).

- RFM: Fixed release of DMA memory buffer (DRVTT-531).

- OP4200: Fixed remote bitstream programming (IOSFP-264).

Version 11.3.2

Features

- RT-LAB: New "Recorders" section in the project explorer and minor GUI enhancements in order to improve the workflow of the data logging system (RTLAB-2213).

- RT-LAB: Added auto-naming feature for data logging files to prevent conflicts (RTLABTT-1151).

- RT-LAB: Signals are now automatically recorded in data logging files when added to a signal group (RTLABTT-892).

- RT-LAB: Added the possibility to delete obsolete recorders through the contextual menu in the project explorer (RTLABTT-855).

- RT-LAB: By default, hide trigger options in data logging configuration (RTLABTT-1146).

- RT-LAB: Added support for MS Visual Studio 2010 x64 (RTLAB-2178).

- RT-LAB: Upgraded WxBase library from 2.8 to 3.0 in order to reduce some controller crashs (RTLAB-2148).

- RT-LAB: New icons for Edition (default) and OP6000 perspectives (RTLABTT-195).

- Added support of Encoder inputs and Encoder outputs on OP4200 system (DRV-2478).

- Added support of Modbus master on OP4200 system (DRV-1857).

- CAN: Added support for CAN-FD communication (DRV-2263).

- MuSE: Added support of programming new bitstreams on remote OP4510, VC707 and OP4200 systems (IOSFP-202).

- IEC61850: Automatically set synchronization state flag when Oregano card is synchronized using 1PPS or IRIG-B (DRV-2649).

- C37.118 slave: Added an option to round the fraction of seconds to emulate perfect timestamp (DRV-2634).

Bugfixes

- RT-LAB: Fixed cases where data logging trigger was inappropriately activated (RTLABTT-1070).

- RT-LAB: Fixed synchronization issues between signals recorded by data logging system and variable table view (RTLABTT-875, RTLABTT-1041, RTLABTT-1094, RTLABTT-1211).

- RT-LAB: Corrected transfer and conversion to MAT/CSV of data logging files when there are several subsystems (RTLABTT-1044, RTLAB-2179).

- RT-LAB: Made conversion to MAT/CSV of data logging files more robust (RTLABTT-1055).

- RT-LAB: Corrected 'Load configuration' operation for data logging information (RTLABTT-984).

- RT-LAB: Fixed Get parameter function which may not read latest value from the model in some conditions (RTLABTT-757).

- RT-LAB: Fixed OpPlotFile block in order for signal names to be present in file header. This assures compatibility with DINAMO (RTLABTT-1111).

- RT-LAB: Forced 'RTWVerbose' option to 'on' to prevent errors in code generation (RTLABTT-1202).

- RT-LAB: Forced 'GRTInterface' option to 'on' to prevent errors in creation of console subsystem (RTLABTT-1027).

- RT-LAB: Fixed retro-compatibility of connection information in projects made with older versions of RT-LAB (RTLABTT-1167).

- RT-LAB: Fixed 'Cancel' button in 'Load configuration' pop-up (RTLABTT-1143).

- RT-LAB: Spaces are now allowed in the name of project configurations (RTLABTT-625).

- RT-LAB: Fixed issue when opening configuration editor for certain projects (RTLABTT-762).

- RT-LAB: Fixed 'Rename' operation for I/O interfaces (RTLABTT-1205).

- ePHASORsim: Fix pins for three-phase voltage source (EPTT-63).

- ePHASORsim: Bus validation logic and error logs (EPTT-68).

- Modbus master: Fixed segmentation fault occurring in RTU mode when no slave is connected (DRV-2629).

- IEC61850: Fixed ICD parser for multiple IEDs per file (DRV-2672).

- DNP3 slave: Fixed the retrieval of the analog/binary event modes (DRVTT-491).

Improved Documentation and Error Reporting

- RT-LAB: Added new example project that explains how to use data logging system (RTLABTT-916).

- RT-LAB: Added verification on 'separate.exe' before model separation and explicit error message (RTLABTT-1138).

Version 11.3.1

Features

- Added support for Modbus master driver

Bugfixes

- Fixed crash when using DINAMO Parameter estimation (RTLABTT-942)

Version 11.3.0

Features

- RT-LAB: New data logging system with continuous and triggered recording capabilities (RTLAB-1536).

- RT-LAB: New acquisition source in ScopeView for new data logging system (RTLAB-1536).

- RT-LAB: New "data" folder in project explorer in order to easily access recorded simulation data (RTLABTT-870).

- RT-LAB: New "scripts" folder in project explorer for editing and executing Python scripts (RTLABTT-650).

- RT-LAB: Support of Simulink SLX file format (RTLAB-1959).

- RT-LAB: Support of Simulink dashboard blocks for prettier console subsystems (RTLAB-1959).

- RT-LAB: New RT-LAB logo! (RTLAB-1959).

- RT-LAB: New license file is needed for OS verification (RTLAB-2134).

- RT-LAB: At load of model, the active view is "Display" instead of "Variable Table" (RTLABTT-385).

- ARINC-429: Added new dynamic driver interface for Abaco PCIe card (DRV-2044).

- DNP3 slave: Added support of the new configuration interface (DRV-2335).

- DNP3 master: Added support of the new configuration interface (DRV-2336).

- MuSE: Added support of OP5707 and OP4510 as central systems (IOSFP-270).

- MuSE: Added MAC address management for remotes OP4200 (IOSFP-215).

- ePHASORsim: Single cage and double cage induction generator (EP-1164).

- ePHASORsim: Adjustable (internal voltage and impedance) 3-phase voltage source (EP-1250).

- ePHASORsim: New version for Excel template (V1.6) and new components (EP-1087).

- ePHASORsim: Multiphase transformer for distribution systems (EP-1173).

- ePHASORsim: A new example (PHASOR-22) with induction generators (EP-1165).

- ePHASORsim: Detailed report about partitioning if number of partitions is greater than 1 (EP-1167).

Bugfixes

- RT-LAB: Better performance when setting parameter values with API functions (RTLAB-2055).

- RT-LAB: Better performance when creating aliases on OpInput and OpOutput blocs (RTLABTT-880).

- RT-LAB: OpenProject API function works in multi-thread or multi-process context (RTLABTT-681).

- RT-LAB: Negative time factors in Load and Execute API functions are forbidden (RTLABTT-619).

- RT-LAB: Setting embedded mode no longer returns "Unable to create embedded simulation" error (RTLABTT-606).

- RT-LAB: Embedded mode works with models without SC subsystem (RTLABTT-792).

- RT-LAB: Fixed several issues when saving or loading project configurations (RTLABTT-751, RTLABTT-940, RTLABTT-755, RTLABTT-876, RTLABTT-723).

- RT-LAB: Restoration of active project configuration is now possible in case of crash (RTLABTT-814).

- RT-LAB: Fixed Controller crash when it is unable to communicate with a model (RTLABTT-776).

- Opal-RT Boards: Renamed the board types in the drop down list to have a more intuitive meaning (DRV-2539).

- ePHASORsim: Including the impact of multiphase shunt status in power-flow (EPTT-51).

- ePHASORsim: Fix in CYME converter for susceptance units (uS as opposed to S) for Overhead Balanced Lines when converting to a multiphase network (EPTT-45).

Improved Documentation and Error Reporting

- RT-LAB: Added documentation for OpenProject and CloseProject API functions (RTLABTT-222).

- RT-LAB: Updated obsolete "Model not specified by previous OpalConnect or OpalSetCurrentModel" error message (RTLABTT-340).

Deprecation and Removals

- RT-LAB: Removed obsolete third-party I/O blocs (Acromag IP, Brandywine PCI SyncClock32, Concurrent FBSSync, NI PXI/PCI-7831, Quanser Q8, SBS Technologies IP) (RTLAB-2128).

- RT-LAB: Support of MATLAB R2011b is deprecated. It will be abandoned in RT-LAB 11.4 (RTLABTT-772).

- RT-LAB: Support of Python 2.2, Python 2.3, Python 2.4, and Python 2.5 is deprecated. It will be abandoned in RT-LAB 11.4 (RTLABTT-781).

- RT-LAB: SetCurrentModel, ConnectByName, and Disconnect API functions are deprecated (RTLABTT-221).

- ePHASORsim: In Excel V1.6 these components are obsolete and must be replaced by their corresponding multiphase pairs: Line 3-phase, Load 3-phase, Shunt 3-phase, Bus Faults 3-phase.

Version 11.2.3

Features

- RT-LAB: Improved the delay when creating a connection to LabVIEW panels when the model is running (RTLABTT-557).

- ePHASORsim: Import three-winding transformer from PowerFactory.

- ePHASORsim: Added new example with a 2000 bus synthetic network (PHASOR-20).

Bugfixes

- RT-LAB: Fixed quality issues with the Controller that manages the targets (RTLABTT-636).

- RT-LAB: Fixed quality issues with the embedded mode (RTLABTT-598, RTLABTT-606).

- RT-LAB: Fixed project configuration pop-up when parameter values change (RTLABTT-621).

- RT-LAB: Fixed conflict between the LoadParameters function and the Variable Table (RTLABTT-640).

- RT-LAB: Fixed a compilation issue with Stateflow models (RTLABTT-660).

- RT-LAB: Fixed a registry key conflict between MATLAB R2011a and R2011b (RTLABTT-653).

- RT-LAB: Fixed dependency of launch sequence on LabVIEW run-time engines (RTLABTT-590).

- RT-LAB: Fixed hanging of the RT-LAB.exe process at close of program (RTLABTT-544).

- RT-LAB: Fixed the appearance of the "Build configurations" window when there is no development node. (RTLABTT-160).

- ePHASORsim: Fixed for *.DZ file in PHASOR-17 example.

- ePHASORsim: Revisions for *.DGS and *.PDF files in PHASOR-17 and 19.

- ePHASORsim: Corrections for project paths for RT-LAB import.

Version 11.2.2

Features

- RT-LAB: Added support for MATLAB R2017a.

- RT-LAB: Added possibility of editing parameters when the model is not loaded. Parameter values can be saved in project configuration (RTLAB-1880).

- RT-LAB: Added support of new bitstream names (RTLABTT-470, RTLABTT-485).

- RT-LAB: Added OS license (RTLAB-1890).

- RT-LAB: Added a "Show in project explorer" option from a LabVIEW panel (RTLABTT-498).

- RT-LAB: Added Lock project mode (RTLAB-1882).

- RT-LAB: Added version number to libraries and executables (RTLABTT-372).

- RT-LAB: Added file mode in signal generator I/O (RTLAB-1885).

- RT-LAB: Added a single scope panel in the "New RT-LAB Panel" wizard (RTLABTT-456).

- RT-LAB: Added Visual Studio Code as a debugging tool (RTLAB-1903).

- RT-LAB: Added data logger synchronous mode (RTLAB-1920).

- RT-LAB: Added data logger automatic file transfer (RTLAB-1809).

- RT-LAB: Added possibility of converting data logger file (.oprec) to .csv or .mat (RTLAB-1929).

- RT-LAB: Improved Simulink error management (RTLABTT-268).

- RT-LAB: Improved RT-LAB installer in order to have a single file (RTLAB-1894).

- RT-LAB: Improved default columns in Variable Table (RTLAB-1918).

- C37.118 master: Added support of the new configuration interface (DRV-2108).

- IEC 60870-5-104 slave: Added support of the new configuration interface (DRV-2210).

- IEC 60870-5-104 slave: Added support of RMS calculation for floating point outputs (DRV-2094).

- OP4200: Added support of 1GHz CPU (DRV-2151).

- OP4200: Added support TSD inputs and TSD outputs (DRV-2230).

- Profibus: Added support of master and slave interfaces (DRV-2190).

- OP5368: Added support of card (DRV-2251).

- I/O SFP: Added partial support for remote I/Os controlled by SFP (DRV-2224).

- ePHASORsim: Added import from PowerFactory DGS file supports FMU.

- ePHASORsim: Added import from CYME is extended to support multiphase transformer, synchronous generator, PV.

- ePHASORsim: Added new example for Microgrid with PV integration as FMU(PHASOR-18).

- ePHASORsim: Added new example for PowerFactory input files with FMU (PHASOR-19).

- ePHASORsim: Added new FMU based components are added, check the user guide to see the complete available items.

- ePHASORsim: Improved impedance of Pi-Line in positive sequence can be tuned during simulation.

- ePHASORsim: Improved bug fix for FMUCreator on Windows 10.

Bugfixes

- RT-LAB: Fixed restoration of connections and aliases when a bus structure is modified (RTLABTT-425).

- RT-LAB: Fixed some API functions that do not return errors (RTLABTT-428).

- RT-LAB: Fixed wrong detection of LabVIEW run-time engines on a 32-bit Windows PC (RTLABTT-494).

Deprecation and Removals

- RT-LAB: Removed the possibility of saving the project configuration when the model is loaded.

- RT-LAB: Removed OpalNode and transfered its functionality to MetaController and OpTargetD (RTLAB-1895).

- RT-LAB: Removed MATLAB embedded view from RT-LAB (RTLABTT-433).

Version 11.2.1

Features

- RT-LAB: Added support for MATLAB R2015b to MATLAB R2016b and partial support for MATLAB R2017a. *Note that Artemis, RT-Events and eFPGAsim are not compatible with MATLAB R2017a.

- RT-LAB: Added support of mixed SignalGroup with and without trigger in Datalogger (RTLAB-1755).

- RT-LAB: Added option to edit the default number of samples per signal in ProbeControl.

- RT-LAB: Improved configuration workflow (RTLAB-1870).

- RT-LAB: Improved OP6000 mode launch and I/O cards icons (RTLAB-1780 RTLAB-1883).

- RT-LAB: Improved RT-LAB blocks documentation (RTLABTT-2 RTLABTT-371).

- CAN: Added support for multiple Kvaser cards in the same system (DRV-2109).

- C37.118 master: Added option to run the driver on a dedicated core (DRV-2105).

- IEC 61850: Added support to run the driver on Windows (DRV-2128).

- IEC 61850: Added option to control the simulation flag and to retrieve both simulation flag and test bit (DRV-2129).

- IEC 61850: Added option to enable all Sampled Values and GOOSE transmission/recepption by default at the beginning of the simulation (DRV-2129).

- IEC 61850: Added support for fixed-length encoding of GOOSE messages as per IEC 61850-8-1 Ed.2 A.3 (DRV-2129).

- EtherCAT master: Added support of EL3161 module.

Bugfixes

- RT-LAB: Fixed eHS automatic connections with OP4200 (RTLABTT-355).

- RT-LAB: Fixed loss of connections and options after renaming a LabVIEW panel (RTLABTT-423 RTLABTT-424).

- RT-LAB: Fixed offline use of OpInput block (RTLABTT-422).

- RT-LAB: Fixed project explorer not showing OpInput and OpOutput folders (RTLABTT-352).

- RT-LAB: Fixed shortcuts removal after uninstalling RT-LAB (RTLABTT-468).

- RT-LAB: Fixed issue with GUI button when switching to embedded mode (RTLAB-1437).

- RT-LAB: Fixed RT-LAB DINAMO license checking (RTLAB-1878).

- RT-LAB: Fixed issue with 2 Matlab process during compilation (RTLABTT-225).

- OP4200: Fixed driver initialization order to allow CAN driver to run with Opalboards driver.

- OP4510: Replaced example model bitstream to include a fix on TSD inputs (DRVTT-133).

- C37.118 slave: Fixed issue with 50Hz nominal frequency (DRVTT-206).

- C37.118 slave: Fixed binding with a specific network interface (DRV-2154).

- C37.118 slave: Fixed use of loopback and wlan network interfaces (DRV-2158).

- C37.118 master: Fixed timeout when stopping the simulation (DRV-2172).

Version 11.2.0

Features

- RT-LAB: Added aliases in RT-LAB.

- RT-LAB: Added aliases, panels and scripts to rtdemo examples (RTLAB-1833).

- RT-LAB: Added new system to protect connections and alias from loss when moving or renaming block in model.

- RT-LAB: Added Import / export workspace (RTLAB-1773).

- RT-LAB: Added new templates in panels section (RTLAB-1853).

- RT-LAB: Added variable table visible when execute model (RTLAB-1819).

- RT-LAB: Added possibility to run TD2.8 scripts (RTLAB-1765).

- RT-LAB: Added the creation of connections in the API (RTLAB-1812).

- RT-LAB: Added error messages when a connexion is refused (RTLAB-1812).

- RT-LAB: Added possibility to display captions or labels in LabVIEW panels (RTLABTT-336).

- RT-LAB: Added LabView panels accessible by default.

- RT-LAB: Added new TestDrive projects.

- RT-LAB: Added Save / Load configuration.

- RT-LAB: Added possibility to delete a configuration (RTLAB-1855).

- RT-LAB: Added Save / Load parameters from GUI.

- RT-LAB: Added TestDrive perspective.

- RT-LAB: Added DataLogger to RT-LAB.

- RT-LAB: Added Driver cores protection from being reserved multiple times in multi-subsystem models.

- RT-LAB: Improved configuration handling for OP6000 projects (RTLAB-1816).

- RT-LAB: Improved RT-LAB clean option at startup (RTLABTT-177).

- RT-LAB: Improved RT-LAB uninstaller (RTLAB-1812).

- RT-LAB: Updated EULA licence Intel.

- RT-LAB: Updated variable table and API to update with LabView widgets.

- CAN: Added new solution with support of CANdb parsing, bit-aligned signals and display of message content.

- CAN: Added cyclical messages support to Kvaser and OP4200 drivers.

- TestDrive: Add support of new hardware based on Linux, OP5142 cards and PCIe communication.

- RFM: Add support of GE 5565-PIORC 256M.

- IEC61850: Improved timing precision when transmission is synchronized by Oregano card.

- Pickering: Added support of 50-295-021-5/12 resistive card.

- C37.118 slave: Initialize timestamp to system time when using local synchronization source.

- C37.118 slave: Added support of simulation mode on Windows system.

- Synchronization: Added support of new profiles on PTP mode.

- OP4200: Added support of OPC-UA server interface.

- ePHASORsim: Import from PowerFactory DGS file is added (built-in balanced system).

- ePHASORsim: Import from CYME is extended for balanced system (built-in and FMU components).

- ePHASORsim: Import from CYME is extended to support ECG, distributed loads, and voltage regulator, recloser .

- ePHASORsim: Import from PSS/e is extended to include HVDC (as FMU).

- ePHASORsim: Power-flow supports multiphase components.

- ePHASORsim: Power-flow has Flat Start and Smart Start for initial guesses.

- ePHASORsim: Import from CYME can now use the internal power-flow option instead of CYME's power-flow Excel file.

- ePHASORsim: New demos are added for test automation, modified WECC system, PowerFactory and CYME input files.

- ePHASORsim: Set number of cores to 1 on linux machine if EPHASOR_THREADS is not defined.

- ePHASORsim: PQ measurement outgoing pins are added to multiphase lines.

- ePHASORsim: License update is required to Version 2017.5.

- ePHASORsim: Check Migration Notes in the user guide for mandatory changes.

Bugfixes

- RT-LAB: Fixed get value of vector elements always return value of first element (RTLABTT-348).

- RT-LAB: Fixed API function GetActiveModels (RTLABTT-361).

- RT-LAB: Fixed support of 3x3 matrixes (RTLABTT-270).

- RT-LAB: Fixed support of multiple connexions to the same controller (RTLABTT-188).

- RT-LAB: Fixed 1st RT-LAB opening problem with Windows 10 (RTLABTT-213).

- RT-LAB: Fixed compilation for models with fixed-point type (RTLABTT-171).

- RT-LAB: Fixed asynchronous process with gcc (RTLABTT-140).

- Orchestra: Fix stability issues.

- IEC61850: Fix order of data attributes in GOOSE message.

- ePHASORsim: Bug fixes for constant current load.

Deprecation and Removals

- RT-LAB: Removed Infiniband link (RTLABTT-144).

Version 7.3.2

Features

- Compatibility with RT-LAB 11.3.2

- New TSB model (TSB-RD) 2-level

- New TSB model (TSB-RD) 3-level NPC (2 and 3 phases)

- New TSB model (TSB-RD) 3-level T-type (RD stands for real diodes)

- Note: previous TSB models are still available

- Improved switch matrix permutation calculation speed in offline mode and in RT-LAB model separation.

Improved Documentation and Error Reporting

- New TSB-RD demo section in ARTEMiS on-line demos

- New application note: How to decouple a model

- New application note: Switch models in ARTEMiS

- New application note: How to adjust RC snubber for TSB

- New application note: About Park Transforms

- New application note: LU vs LDLt factorizations in SSN

- New Application Note section in ARTEMiS Demos (under Scientific paper and benchmark section)

- Online Demos reorganized to be unique across matlab versions and placed in the common folder of the installation

- Added some papers and PPT in ARTEMiS scientific paper section.

Version 7.3.0

Features

- Compatibility with RT-LAB 11.3.0 and with RT-LAB 11.3.1

- SSN synchronous machine block with backward Euler option

Bugfixes

- SSN OLTC blocks: small correction in no saturation mode made to allow compilation to complete

- 3-level NPC demo: correction to allow DC bus to charge correctly considering null initial conditions

Improved Documentation and Error Reporting

- New paper on SSN rotating machine included in examples section

- New application notes section in examples section

Version 7.2.3

Features

- Compatibility with RT-LAB 11.2.3

- Renamed "SSN Ground Referencing Resistor" block.

Bugfixes

- Fixed certain RT-LAB compatible online demos: ssn_9LevelDrive_xfozigzag, ssn_DFIM_wind_turbine_with_crowbar and SSN_IEEE_123Node.

- Correction to SSN resistance model.

Improved Documentation and Error Reporting

- Added documentation for Artemis decoupling blocks and editable sample time.

Version 7.2.2

Features

- Compatibility with RT-LAB 11.2.2

- Compatibility MATLAB 2011b, 2015a-SP1 (prefered version), R2016b, R2017a (64 bits)

- SSN solver and discretization methods are now used for all electric subsystems, even if the model is not modeled with SSN (flag DISABLE_SSN_FOR_NON_SSN_MODELS can be used to use old state-space S-function)

- SSN initial conditions now set to 0 automatically

- New Kundur 4-machine, 2-area model with SSN synchronous machine

- SSN printout of matrix inversability condition number when USE_MFILE_SSN_SFUNCTION=1 is set in workspace

- Updated 3 winding 3-phase OLTC transformer demo using SSN: now without S-function builder block.

- 3-level NPC TSB model: ground connections are now implicit.

Bugfixes

- Code correction in SSN-OLTC model v2 (without S-function)

Improved Documentation and Error Reporting

- Added scientific paper section to the demos

- Added benchmark section to the demos

- New IEEE 123 node test feeder using SSN demo

- Bipolar HVDC with switched filter banks online demos modified to have better numerical response with LDLT solver.

- New SSN demo containing distributed parameter line with breakers and faults at both ends

Version 7.2.1

Features

- Compatibility with RT-LAB 11.2.1

- RT-LAB snapshot functionality for Simscape Power Systems sfun_discreteVariableDelay S-Function. This allows support for the following blocks: in powerlib_meascontrol/Measurements: Fundamental(PLL-Driven), Mean(Variable Frequency), Positive-Sequence(PLL-Driven), Power (PLL-Driven, Positive-Sequence); and also in powerlib_meascontrol/PLL blocks.

Improved Documentation and Error Reporting

- Major scientific papers at ARTEMiS-SSN now accessible in the on-line demo section

- SSN benchmarks accessible in the on-line demo section

- Various small corrections to demo models

Version 7.2.0

Features

- Compatibility with RT-LAB 11.2

- Compatibility MATLAB 2011b, 2015a-SP1 and R2016b (prefered versions)

- New LDLT Factorization option in SSN to improve real-time speed.

- Adding Delayed Speed Term option in most SSN rotating machine models (SM, DFIM and PMSM)

- Model updates for SSN-SM: more measurements available

- New SSN Custom models available: Parallel RLC, Series RLC, R, all with on-line changeable RLC parameters.

- Quadruple precision precalculation in SSN using op_ssn_online_quad_precision_inversion workspace variable. This flag makes ARTEMiS precalculation routine uses quadruple precision floating point arithmetic for all matrix inversions, on the target only. Windows and Microsoft Visual Studio donâ€™t support quadruple precision, therefore the option will only have an effect during real-time simulation on Linux targets.

- New Reconfigurable breaker model available with script and demo. Using this model, one can turn breakers into fixed/closed circuits using a single model running multiple test scenarios.

- Removal of iteration printouts by default in offline mode. op_ssn_print_iteration_info variable must be set in workspace now.

Bugfixes

- Major bug correction for SSN solver affecting Rotating machine models mainly: the model admittance matrix was copied in the global system admittance matrix in a transposed way. The copy of the admittance matrix is now correctly done. This only affect machine models, without delayed speed terms, because these have asymetric matrices.

- Model corrections to SSN-SM and SSN-DFIM to have a delayed discrete B matrice used during SSN model calculation. This delayed B matrice corrects a discrepency between internally computed current and external ones in case with machine connected to very small loads.

- Installer correction: IEEE 39 bus 10 machine demo is now really accessible

Improved Documentation and Error Reporting

- HELP available for iMOV, TSB 2-level, TSB 3-level and other blocks

- SSN Dynamic load demo available. More stable that injection-based dynamic load of SPS. (beta version)

- New RT-LAB and ARTEMiS SSN Monte-Carlo test demo using snapshot feature

RT-EVENTS

Version 4.3.2

Features

- Provided compatibility with RT-LAB 11.3.2.

Version 4.3.0

Features

- Provided compatibility with RT-LAB 11.3.0 and RT-LAB 11.3.1.
- RT-LAB snapshot supported for all RT-EVENTS blocks

Version 4.2.3

Features

- Provided compatibility with RT-LAB 11.2.3.

Version 4.2.2

Features

- Provided compatibility with RT-LAB 11.2.2.

Version 4.2.1

Features

- Provided compatibility with RT-LAB 11.2.1.

Version 4.2.0

Features

- Provided compatibility with RT-LAB 11.2.0.

- Added support for MATLAB versions R2015b, R2016a, R2016b and R2017a, including support for 64 bit versions.(EMSTT-53)

Bugfixes

- Fixed bug where rte_scope crashes during offline 64 bit Simulink simulation.(EMSTT-52)

- Fixed bug in rte_filter where rise time and fall time occur in consecutive calculation steps, and time between them is shorter than the filter pulse width. Rise was incorrectly moved to start of its calculation step. Now rise time is correctly moved to start of the next calculation step which also contains fall time.(EMSTT-48)

- Fixed bug introduced in version 4.1.4 that caused offline simulink simulations that contained rte signals to crash.

Version 1.5.4

Features

- Added standard motor package for OP5700 (EFS-1667)

- Added demos for eHS with PMSM with and without I/Os for OP5700 (EFS-1870)

- Added demos for eHS with DFIM with and without I/Os for OP4510 and OP5700 (EFS-1890, EFS-1886)

- Added demos for eHS with SCIM with and without I/Os for OP4510 and OP5700 (EFS-1889, EFS-1887)

- Added demos for eHS with SRM with and without I/Os for OP4510 and OP5700 (EFS-1891, EFS-1888)

- Added demo for a eHS with PMSM SH and IOs for OP4510 (EFS-1919)

- Added standard motor package for OP4510 with Kintex-7 410t (EFSTT-265)

- Added time-stamped T-Type converter feature to use with eHS (EFS-1987)

- Added two inputs dot product feature to use with eHS (EFS-1987)

Bugfixes

- Fixed netlist creation issues when using both Lca and non-Lca switches in same circuit model (EFSTT-237, EFSTT-269)

- Fixed a bug preventing from using multiple inverter solver blocks with different parameter sets (EFSTT-202)

- Fixed Sine Wave Generator output mapping issue (EFSTT-158)

Version 1.5.3

Features

- Added official support of Matlab versions 2015b, 2016a, 2016b and R2017a

- Performance improvement of eHS during update and build of the CPU model (EFS-1177)

- Added standard motor package for OP4510 (EFS-1671)

- Added official support for OP4200 1GHz (EFS-1843)

- Added demo for a eHS with PMSM and IOs for OP4510 (EFS-1687)

- Added OP4510 eHS with machine firmware (EFS-1685)

- Added support for eHSx128 in eFPGASIM XSG library (EFSTT-85)

- Added XFO support in PLECS (EFS-463)

- It is now possible to change the Flux value of the PMSM VDQ block on the fly (EFS-1797)

- Added support of eHS circuits without state (EFSTT-4)

- Added support of *.xlsx file format to the eHS Scenario feature (EFSTT-40)

Bugfixes

- Fixed AOMR Jitter issue (EFSTT-18)

- Fixed typo in eHSx32 for OP4200 mask (EFSTT-131)

- Fixed mixed up results for Thermal Losses when increasing the number of converters (EFSTT-160)

- Fixed issue when changing the number of external inputs of eHSx128 (EFSTT-163)

Deprecation and Removals

- Removed the eHS Gen2 CommBlk from library (EFSTT-178)

- Removed MMC Example models from available demos

Version 1.5.2

Features

- Added Beta support of Matlab versions 2015b, 2016a and 2016b. (EFS-1457)

- Added the loss calculation module for 2-level bridges of eHS (EFS-1109)

- Added the option of "eHSx128 + custom field" in the AOMR console block (EFS-1465)

- Added support of firmware generation with eHSx128 (EFS-1175)

- Added a monitoring feature to evaluate the local min and max of eHS outputs for a CPU time step (EFS-1170)

- Added a monitoring feature to evaluate the instantaneous Power (V*I) by using eHS outputs (EFS-1101)

- Added led and RS422 port support for OP4510 standard firmware (EFSTT-68)

Bugfixes

- Fixed a bug related to eHS output average calculation that was saturating to 255 samples (EFSTT-17)

- Fixed a bug that prevent from using multiple PMSM machine blocks at the same time in the same CPU model with different parameters (EFS-1466)

- Fixed bugs in circuit parsing (SimPowerSystems workflow only) (EFSTT-37 - EFSTT-25)

Version 1.5.1

Features

- Added support for the eHSx128 form factor in the eHS Gen3 CPU block. (EFSTT-36)

- Added RT-LAB eHSx128 Gen3 example model. (EFS-775)

- Added support of circuits containing more than 72 switching elements using eHSx128 Gen3 form factor (EFSTT-3)

- Added support of circuits containing more than 32 sources using eHSx128 Gen3 form factor. (EFSTT-7)

- Updated the Analog Output Mapping and Rescaling console block to support eHSx128 Gen3. (EFS-994)

- Added error handling for 0 or infinite R, L, or C values. (EFS-998)

- Added support for PSIM and PLECS circuit models on the OP4200 platform. (EFSTT-48, EFSTT-52)

- Added support for eHS OP4200 eHS Block to automatically detect if the circuit model has changed. (EFS-925)

- Added T-type sub-module MMC (MMC5) as a separate block in the library, still maintain MMC4 product. The gating signals from CPU definition has changed.

Bugfixes

- Fixed bug with Selectable Digital Inputs not working correctly on all targets. (TT-8978)

- Fixed eHS parsing errors that could occur with certain combinations of Two-Level and\or Three-Level switches. (EFSTT-23)

- Fixed behavior of Cancel button in the OP4200 GUI for eHS. (EFS-902)

- Fixed error with the OP4200 eHS Block when the minimum eHS time-step was larger than the maximum eHS time-step. (EFS-916)

- Fixed issue in the eHS OP4200 eHS GUI related to the naming of Two-Level and Three-Level switches when placed in separate subsystems. (EFS-925)

Improved Documentation and Error Reporting

- Updated eHS Quickstart Guide, updated User Guide, and created OP4200 Quickstart Guide (EFS-776, EFSTT-36, EFS-775)

Version 1.5.0

Features

- Added eHSx32 support on the new OPAL-RT platform: OP4200.(EFS-424)

- Introduced a new and improved GUI for eHS on OP4200 which is accessible via the Simulink library block for eHSx32 on OP4200.(EFS-424)

- Added an example project for OP4200 which consists of a boost with a two level inverter.(EFS-845)

- The Analog Output Mapping and Rescaling console block was updated to improve usability and support for future eHS form factors. (EFS-856)

- Introduced BETA version of eHSx128 form factor in eHS Gen3 CPU block. (EFS-481)

- Updated MMC demos to fix a display issue in MATLAB 2014b (moved the calculation units from SC_Console to SM_Subsystem).

Bugfixes

- Fixed issues related to source naming when source is contained in subsystem. This may now affect order of inputs in models build with earlier version of eFPGAsim. (TT#8968)

- Fixed an issue with glitches in the DC voltage for MMC running on a slave FPGA. (TT#8967)

Improved Documentation and Error Reporting

- Updated MMC training slides to include software version information and compatibility.

Version 1.4.3

Features

- Removed the dependency to RT-XSG libraries in MMC FPGA models.(TT#8894)

- Added support for MMC models in different types of FPGAs: VC707_2, MMPK7_325T and TE0741_325T.(TT#8895)

- Added standardized SFP drive in MMC model in FPGAs V7, MMPK7_325T and TE0741_325T.(TT#8896)

- Modified MMC4 black box source code to improve the accuracy inside MMC. (TT#8897)

- Set bitstream of MMC demos in the intial files automatically using 'efsSetBitstreamFile.m'.(TT#8898)

- Added masks and documentation for the RT-XSG blocks for Dual PMSM-VDQ, Induction Machine, Angle Sensors. (TT#7638)

- Added a firmware bitstream pool directory in the Matlab path accessible by all RT-LAB models, including eFPGAsim example models. (EFS-387)

- Updated the eHS models "Two-Level Inverter" and "Three-Phase Diode Bridge" to eHSx64 Gen3 for all platforms. (EFS-395)

- Added support for SLX files for circuits designed with the SimPowerSystems and PLECS toolboxes. (EFS-402)

- Modified eHS with IOs example models to include the RT-XSG Selectable DIO blocks and . (EFS-450)

- Added support for the Loss-Compensation Algorithm for eHS for circuits designed with PLECS. (EFS-457)

- Added support for thyristors for eHS for circuits designed with PLECS. (EFS-465)

- Added support for .CCT files for circuits designed with PSIM. (EFS-488)

- Modified the eFPGAsim toolbox installer to prompt the user for administrative rights for automatic installation within the Matlab path. (EFS-511)

- The eFPGAsim JAVA packages are now installed in the Matlab static JAVA class path. (EFS-517)

- Added support for PLECS and PSIM circuit editors in the "Two-Level Inverter" and "Three-Phase Diode Bridge" example models. (EFS-537)

- Modified eHS with IOs example models to include a generic Analog Output solution (handling both the static analog outputs and the Analog Output Mapping and Rescaling function). (EFS-611)

- Added a security check in the eHS Gen3 solver to prevent the user to enter a custom solver step size outside the range available for the solver. (EFS-676)

- Added support for multiple 3-level bridges in a circuit simulated using the eHS solver. (EFS-737)

- Seperate the library in 2 library in the library browser (eFPGAsim and eFPGAsim XSG). (EFS-762)

- Added an option to the eHS Gen3 CommBlk to enable an automatic communication port management that works for most firmware configurations. (EFS-763)

- Added support for three-phase measurement blocks for circuits designed with the SimPowerSystems toolbox. (EFS-764)

- Added support in eHS for circuits designed with PSIM 10.0.6. (EFS-765)

Bugfixes

- Fixed issue with MMC demos not being able to run in MATLAB 2014b. (TT#8893)

- Fixed an issue with the eHS Gen3 solver preventing the outputs to be updated when the measurement count is equal to 1, 9, 17 or 25. (TT#8768)

- Fixed an issue with the RTXSG Scope and FPGA 64-to-64 Interconnect control panels channel selection set by the block causing the selection to reset every time the Simulink model is loaded. (TT#8772)

- Fixed an issue preventing the correct switch control mapping for FPGA-based PWM Generators (TT#8812)

- Fixed an issue in the eHS Gen3 CommBlk causing the "RTE Gates" setting to reset when the model is re-opened. (TT#8814)

- Fixed an issue with the Analog Output Mapping and Rescaling Control Panel causing the last available signal not to appear in the signal selection drop-down list for each output channel. (TT#8816)

- Fixed an issue with the eHS scenarios causing all outputs to fall to zero when using an non declared scenario. (TT#8817)

- Fixed an issue with the Dual PMSM-VDQ controller block (CPU side) causing a scaling error on the Idq axis of the Ld-Lq tables while using the Standard park transform. (TT#8868)

Deprecation and Removals

- Removed support for Xilinx ISE Design Suite for eHS with IOs example models for OP4500, OP4510 and OP5607. (EFS-761)

Version 1.4.2

Features

- Support of Matlab R2015a SP1. (EFS-361)

- Support of eHSx32 Gen3 for smaller FPGA boards (OP4200 / OP5600 / OP7161). (EFS-341)

- Support of Thyristor (PSIM and SimPowerSystems circuit editors). (EFS-353)

- Support of LCA in PSIM (using the VSI block). (EFS-373)

- Support of PLECS 3.7. (TT#8732)

- Beta support of PSIM 10 (requires a PSIM patch). (EFS-354)

- Implemented new VSC controller in MMC-HVDC CPU and MMC-HVDC FPGA demo models.

- Added over-current protection to MMC-HVDC FPGA and MMC-HVDC-DUO FPGA models.

- Added over-voltage protection reset function to MMC FPGA blocks in the library and 4 FPGA models.

Bugfixes

- Fixed a bug that prevents "AinDin_AdjustmentsAcquisition" block from updating properly. (TT#8733)

- Fixed a bug that caused a JAVA error while using eHS on with regional settings of Windows 7. (TT#8745)

- Fixed a bug that caused an error during parsing the switches of a PSIM circuit for a large switch number. (TT#8747)

- Fixed a bug in PMSM-SH v2 block where machine 1 dq transforms parameters were not applied properly. (TT#8746)

Deprecation and Removals

- Removed the support of Matlab R2010b. (EFS-385)

- Removed the support of QNX. (EFS-368)

Version 1.4.1

Features

- Added support for RT-XSG v3.0+ in eFPGAsim, including porting the support for firmware generation using the Xilinx Vivado Suite and Matlab R2014b. (TT#8663)

- Example models "Boost and two-level bridge" and "Two-level Bridge" for eHSx64 Gen3 are provided with an OP4510 firmware, and models are configured for OP4510 by default. (TT#8656)

- Updated MMC libraries in FPGA and CPU and the files for generating bitstream for MMC4 with deadtime and overvoltage protection feature. (TT#8657)

- Added support for control of eHSx64 Gen3 inputs from another eHS core. (TT#8658)

- Added support for control of eHSx64 Gen3 inputs from analog inputs. (TT#8661)

- Added a patch to the RT-XSG blocks for the eHS solver and of the Analog Output Mapping and Rescaling function to avoid 'Bool type output port op gets indeterminate value' errors during offline simulation. (TT#8605)

- The eHSx64 Gen3 reset signal (coming from RT-LAB) is now resynchronized with the simulation step pulse (ModelSync). (TT#8664)

- Added 6 example model for the FPGA-based Modular Multilevel Converter (MMC) models to the eFPGAsim demo browser. (TT#8665)

Bugfixes

- Fixed a bug in eHSx64 gen3 that avoided the user of using more than 55 switches. (TT#8696)

- Fixed a bug in dbl2sfp function. Extended mantissa was forced to 0 in some cases leading to wrong simulation results (system time constant was reduced). (TT#8697)

- Fixed an issue causing wires to be disconnected inside one component in MMC library of eFPGAsim version v1.4.0. (TT#8636)

- Corrected the eHS report log to eliminate time-step duration truncation and to fix an incorrect "Solver desired time step" value appearing the first time it is shown after the option "Provide explicit sample time for solver eHS" is unchecked. (TT#8659)

- Corrected the optimal Gs proposed by the Gs Optimization Tool is incorrect for Single-phase Three-level NPC Converter, resistive load to take into account the converter base current. (TT#8660)

- Fixed an issue causing the minimum time step to set to real time step value in circuit info of the eHSx64 Gen3 block. (TT#8634)

- Fixed an issue causing Simulink not being able to change Gate controls from the Gate control selection panel. (TT#8610)

- Fixed an issue with the "Multimeter" block support causing misassignations in the measurement types and names. (TT#8666)

Improved Documentation and Error Reporting

- Added documentation for the Switched-Reluctance Machine (SRM) block. (TT#8632)

- Added a Quickstart Guide for the eHS solver. (TT#8662)

- Added documentation for the Analog Output Mapping and Rescaling (AOMR) block. (TT#8621)

Version 1.4.0

Features

- Added the support of eHS Gen3 with LCA (Loss Compensation Algorithm) for 2-level and NPC converter topologies (SimPowerSystems workflow only). (TT#8594)

- Added the support of LCA in the eHS offline simulation block. (TT#8595)

- Upgraded eHS Gen2 example models to eHS Gen3 for Virtex-7 and Kintex-7 compatible chassis (NPC converter example). (TT#8596)

- Added FPGA PWMo function in the example models that can be mapped to the eHS circuit switches. (TT#7862)

- Added examples model of eHS Gen3 (3-Phase Inverter with Boost and 3-Phase inverter examples). (TT#8596)

- Added a netlist report during eHS Gen3 equation generation. (TT#8597)

- Made a tool to calculate Gs based on the topology (TT#8603)

- Added a GUI to map the gate sources to the netlist switches (eHS Gen3 only). (TT#8601)

- Increased the maximum number of scenarios available for eHS Gen3 (up to 1023). (TT#8599)

- Added the support of Matlab R2012b R2013a R2013b R2014b R2015a (32bits and 64bits). (TT#8598)

- Added a PLL and PID functions for RCP applications. (TT#8553)

- Added a new MMC topology Clamp-Double Sub-module (CDSM). It must be applied with Artemis version v7.0.2.773 and later to realize the functionalities of CDSM in a MMC system.

Bugfixes

- Fixed Unknown error a model was not including a SimPowerSystems POWERGUI or a PLECS circuit. (TT#8602)

- Fixed current measurment are wrong when the ground is present in SimPowerSystems for multi branch measurment. (TT#8504)

- Fixed the compatibility issue between the MMC block callback and RT-LAB 11.0.3. (TT#8600)

Version 0.3.8

Features

- Added example models of eHS with I/Os for OP4510, OP4500 and OP5607. (TT#8543)

- Added support of the PMSM Spatial Harmonic block v2 (Larger tables, embedded mechanical model). (TT#8545)

- Support of SRM block for Virtex-7 and Kintex7-based chassis. (TT#8544)

- Added the support of the "DC link filter + 2 inverters" mode in the inverter solver with boost block. (TT#8546)

- Added FPGA 64-to-64 Interconnect block to eFPGAsim CPU and FPGA libraries. (TT#8552)

Bugfixes

- Fixed RLC and LC component support in the eHS circuit parsing function. (TT#8555)

- Fixed NI Multisim support in eHS. (TT#8306)

- Fixed an issue in the Switched-Reluctance Motor (SRM) block that was causing an initialization error during model compilation. (TT#8557).

Version 0.3.7

Features

- Added a Neutral-Point Clamped (NPC) converter example model for eHSx16 on ML605. (TT#7612)

- Added an example model for eHSx16 with I/O interfaces for ML605. (TT#8520)

- Added a "Selectable Digital Output" block to the HIL I/O library (this block can handle static digital outputs, Event Generator signals and Pulse-Width Modulated digital outputs). Added a "Selectable Digital Input" block to the HIL I/O library (this block can handle static digital inputs, Event Detector signals and Pulse-Width Modulated digital input analysers). (TT#8521)

Bugfixes

- Fixed help link for MMC Pulse block (MMC Gate Control Panel). (TT#8440)

- Fixed an issue with eHSx64 internal sine wave generators requiring the parameters for all 32 sine wave generators to be provided (causing malfunction of the generators if the "Use as many inputs as the current netlist requires" option was selected). (TT#8517)

- Fixed eHSx16 support for mutual inductance element that was causing matrix generation to fail with error "Reference to non-existent field 'value'.". (TT#8518)

- Fixed an issue with the MMC FPGA control block to enable custom OpCtrl or OpLnk controller name. (TT#8523)

Improved Documentation and Error Reporting

- Fixed inconsistencies in the documentation of the Analog Output Mapping and Rescaling block and Inverter Model with Boost block. (TT#7939)

Version 0.3.6

Features

- Added a MMC library that contains a block which has a choice of MMC half-bridge or full-bridge, MMC valve control blocks and 6 MMC demo models in typical Power System applications with related help files. (TT#8509)

- Support of the PMSM Spatial Harmonics solver and Inverter solver on Virtex-7 FPGAs. (TT#8508)

- Support of RL RC elements of PSIM in eHS circuit parser. (TT#8506)

- MMC 3x512: Added the option to choose whether to have faults and gates inputs or not, fixed the behavior when the selection options are unchecked. (TT#8438)

- MMC 3x512: the decimation factor can be obtained when the FPGA is in slave mode,

and the following blocks are now compatible with both OP7020 and OP7000:
- Modular Multilevel Converter with Integrated Controller (3x512 cells)
- Modular Multilevel Converter with Integrated Controller (3x512 cells) (Valve Current and VMMC)
(TT#8476)

Bugfixes

- Bugfix: "Analog Output Mapping and Rescaling block Control Panel" was not working properly when linked to the library. (TT#8507)

- Bugfix: eHSx64 initialization port number was stuck to 1 and impossible to change. (TT#8439)

- Fixed an issue in the OP7161_2-based 3x512-cell Multilevel Modular Converters (MMC) causing wrong Vmmc values in averaged mode. (TT#8425)

- MMC: Fixed the bug of gliches on Vmmc when Vmmc_ave mode is checked when running MMC model with OP7000, obtained different decimation factors when there are more than one FPGA. (TT#8410)

- Fixed incorrect sequencing of capacitor voltages received from OP7161_2-based Multilevel Modular Converters (MMC) models using the 3x512-cell MMC library. (TT#8409)

Version 0.3.5

Bugfixes

- Fix for the conversion function dbl2ssfp43.p that was returning wrong results for input values slightly inferior to powers of 2. (TT#8424)

Version 0.3.4

Features

- Added support for mutual inductances and transformers with both generations of eHS for SimPowerSystems and PSIM workflows. (TT#8420)

- Added support for eHSx64, the second generation of eHS solver. It features a higher computation power (4x), more input/outputs, better accuracy and support for scenarios. (TT#8418)

- Added support for induction machines in the motors library. (TT#8415)

- The second core of the dual eHS was assigned the same configuration and circuit as the first core. They can now be independent. (TT#8304, RT3#276253)

- Added support for the MMC model on the OP7000 generation of simulators. Also added a three-valve, 512-cells-per-valve Modular Multilevel converter block, with new implementation of MMC which removes the parameters to adjust snubber from the previous versions. (TT#8123)

Bugfixes

- Fixed the support of int32 parameters in Ansys data (TT#8417)

- Fixed an issue with the the PMSM SH solver core. The Current results were sqrt(2/3) off the reference results when using the Ansys machine data. (TT#8416)

- Bugfix: the CPU block was keeping the last solver output state when reset. When reset, the solver is outputting 0 on all outputs now. (TT#8371)

Version 0.3.3

Features

- Support of parasitic parallel resistance in the boost inductor (dual inverter with boost block). (TT#8183)

- Add Ansys support in PMSM Solver Spatial Harmonics (TT#8182)

- Support of OP4500/VC707 for motors/converters/IOs/Sensors blocks (TT#8181)

Bugfixes

- Fixed an issue where the Vmmc value would drop by 16 volts when switching to normal mode. (TT#8124)

Improved Documentation and Error Reporting

- Added entry for DeltaT/C in the documentation of the Capacitor Differential Equation Solver block. (TT#8283)

Version 0.3.2

Features

- NaN were inserted in the Ld Lq and flux tables when the breakpoints were not the same for Id and Iq or the breakpoints were not defined for +/- max Iamp value (symmetric around 0). NaN are now replaced by the nearest non-NaN value. (TT#8105)

- The eHS configuration matrix location is now provided with its relative path, enabling the packaging and distribution of pre-compiled RT-LAB projects with the eHS feature. (TT#8076)

- Add support for FGPA based MMC valve and valve control. Requires RT-LAB v10.7.3 or later. (TT#7743)

- Added a 512-cell Modular Multilevel Converter (MMC) Valve and Valve Controller models. Requires RT-LAB v10.7.3 or later. (TT#7743)

- Added the RT-XSG Scope to the eFPGAsim I/O library. This scope enables the monitoring of internal FPGA signals with very fine time resolution (down to 5 ns). (TT#7482)

Deprecation and Removals

- The "2 DC source + 2 Inverters" mode of the Inverter_Solver_wboost block is not supported and returns an appropriate Matlab error the to user. (TT#8111)

Version 0.3.1

Features

- In machine models PMSM-VDQ and PMSM-SH, the Rabc force feature did not operate properly. The equation has been fixed. (TT#8055)

- Added the RT-XSG block for the "Analog Output Mapping and Rescaling" function. (TT#7882)

- Added support for initial states of Capacitor and Inductor in eHS for PLECS. (TT#7880)

Bugfixes

- Fixed an issue in the PMSM-SH machine model related to a 30-step delay between motor 1 and 2 computation not being accepted by the callback despite its being a legal setting. (TT#8054)

- Fixed an issue in the PMSM-SH machine model related to the FPGA interpolation function malfunction causing spikes on the torque. (TT#8053)

- Fixed an issue in the PMSM-VDQ machine: the block did not update properly when motor 2 is used in LdLq table mode. (TT#8052)

- Fixed an issue in the PMSM-VDQ machine model where the flux and back emf amplitude were not right when the user set the LdLq table mode. (TT#8051)

- Fixed an issue with the allocation of communication port numbers of the Dual eHS

block when the linked OpCtrl block was taken from the Opal-RT I/O Common library. (TT#8005)

Version 0.3.0

Features

- Added support for nonzero capacitor initial voltage and inductor initial current in eHS. (TT#7880)

- Added support OP4500 Kintex7-based hardware platform for the eHS solver. (TT#7898)

- Added support for switch control polarity selection (active-high or active-low) in eHS. (TT#7881)

- Added support for AC and DC voltage and current sources in eHS, implemented as embedded source signal generators on the FPGA entity of eHS. (TT#7879)

- Added a very low leakage capacitor model block in the eFPGAsim Elements libraries. (TT#7878)

Version 0.2.4

Features

- Added the 2-Level Inverter with Boost block. (TT#8031)

- Enhanced the eHS solver RT-XSG block packaging and documentation. (TT#7899)

- Added support for OP7020 and OP5607 Virtex7-based hardware platform for the eHS solver and Dual PMSM-VDQ motor model. (TT#7900)

Version 0.2.3

Features

- Added a 24-phase PMSM motor function. (TT#8032)

Version 0.2.2

Features

- Added support for OpLnk controller blocks (in addition to OpCtrl's) for the eHS solver. (TT#7815)

Version 0.2.1

Features

- Added support for PLECS to design the circuits used by the eHS solver. (TT#7759)

- Added the "pulse selection" parameter in the eHS2 solver (a.k.a. "from Din"). (TT#7622)

Version 0.2.0

Features

- Modification of PMSM example model. Links with RT-XSG are now broken. Model can run off-line without RT-XSG installed. (TT#6719)

Bugfixes

- Fixed strange behavior of PMSM torque in motor model. (TT#6749)

- Fixed problem of signal routing when compiling models with 2 motors. (TT#6725)

Version 3.2.1 (Restricted Release)

Features

- Integration of an option to use advanced Xilinx pre-defined parameters for the sub-tools (Tcl commands as "opt_design, map_design, route_design") for increasing the probability of achieving timing closure for tight design/FPGA.

- Multi User System Expansion (MuSE) with flash update support.

- Matlab 2018A support for Vivado 2018.2.

- Vivado 2018.2 support.

- Vivado 2018.1 support.

- New FPGA Artix 7 support (xc7a200tfbg676-3) for OP5600/OP5143 product with 8 mezzanines (no MuSE).

- User clock set to 200 MHz when eHS is detected. (FPGATT-143)

- Implementation of a power down sequence with 7 Series GTX/GTP design for avoiding PCIe loss with VC707. (https://www.xilinx.com/support/answers/59294.html ; FPGATT-130)

- Hardware Configuration and Interconnection Generation improvements. (HCIG; .conf/.opal) (FPGATT-102; FPGATT-183)

- IO Block configuration and name's logic verification improvements. (FPGATT-106/140)

- MuSE - Prevent user from generating a remote bitstream containing eHS block. (IOSFP-349)

Bugfixes

- Script correction for terminating the bitstream generation for the OP4200 with correct name. (FPGATT-165; FPGATT-178)

Version 3.2.0 (Restricted Release)

Features

- Added support for High Speed Link (HSL) for 4 first MGT ports for OP5#707 (the limitation of 4 MGTs is the total of Aurora and HSL). HSL is supported for any port for other product. There is no flash update for remote units.

- Implemented logic to detect eHS block and pops out warning to use 200 MHz if not set. (FPGATT-143)

Bugfixes

- Hardware Configuration and Interconnection Generation (HCIG) bug fixes. (RTXSG-49, RTXSG-68, FPGATT-97)

Deprecation and Removals

- Removed support of MMPK7 (OP4500), end of life.

Version 3.1.10

Bugfixes

- Correction on a bug when changing the hardware configuration. A modification on script opxsgIOBlockUpdate was made to improve the verification of assigned hardware in the model, but the type of the returned value for mezzanine string change whether opening the model or it is aready open.

Version 3.1.9

Features

- OP5607/OP5707 rev.3 support.

- Reinforced OP5342 reset circuitry for removing metastability that might stall the I2C sequencer.

- Applying drive specific strengths for OP5352 and OP5360-2 in Virtex7, Kintex7 and Zynq based systems. (PF317500-6 and PF617539-7)

- Support of the user clock of 200 MHz for the conversion's trigger in the 40 MHz architecture of OP5332. (FPGATT-124)

- Xilinx Vivado 2017.3 and 2017.4 support improvements. (FPGA-78, FPGATT-33, FPGATT-139)

- Support of BiSS-C BETA

- Support of SSI BETA

- Message and configuration improvements - Path length's verification: Not applied to Windows 10 systems. (FPGA-139 and FPGATT-33).

Bugfixes

- Hardware Configuration and Interconnection Generation (HCIG) bug fixes. (FPGATT-97, FPGATT-127)

Version 3.1.8

Features

- Added support for Xilinx Vivado 2017.3 and 2017.4 support with Mathworks Matlab R2017b.

- Added OP5332 (analog OUT @ 2 MSPS) support, added new constraints for OP5342 (Analog IN @ 2 MSPS) and added new clocking domain (64 MHz) for the OP5#07 systems.

- Updated the I2C Sequencer for reading the new IDs of the 126-0308 rev.4.0. Added register address 0x22018.

- EnDat 2.2 bug fixes: Modified the EnDat Master Interface "Ready" manager. Now in VHDL, uses the EC_STATE signal from ENDATREDUCED.

- EnDat 2.2 Master: Added features to prevent the trigger of a EnDat transaction if the previous transaction is not finished or if the bus speed requested "Freq_OEM" is 0 (illegal) or 1 (16 MHz).

- Updated sample RT-LAB models that guides RT-XSG models (buses BusSelector and BusCreator). (RTXSG-63)

- RT-XSG block improvement - Auto-assign 'Direction' to 'Both' when an 'ExpansionSignal' card's 'Type' is selected. (FPGATT-47)

- Synthesis Manager block and Expansion signal block improvements (clock period refresh and direction assignment). (FPGATT-84, FPGATT-47)

Bugfixes

- HCIG (Hardware Configuration and Interconnection Generation scripts) bug fixes and updated documentation (auto .conf and .opal generation). (FPGATT-83, FPGA-89, RTXSG-62)

- OP4200 Zynq @667 MHz (V.1.) and @ 1 GHz (V.2.) Gray Zone selection bug fixes. (FPGATT-81)

Improved Documentation and Error Reporting

- Message and configuration improvements - Correction on error message display for SynthesisManager when updating block; user clock refreshing function. (FPGATT-78, FPGATT-18)

Version 3.1.7

Features

- Added OP5332 support for the OP4510. Updated the Gray Zone with additional clocks and new MMCM port association and updated the interrelated timing constraints. Updated the Version block with additional clocks in the Synthesis Manager block (rtxsg_tools.slx).

- Enforced support for AOMR. Partial support for eHS. Script corrections in nodeToSubsystem.m. Updated script startPoint_tracebackSignal.m : prints the config file's name generated. Modified get_confBlockInfo.m & create_opal_file.m: major modifications for support of AOMR and eHS.

- Added support of EnDat 2.2 rotative protocol communication (Master and Slave).

- OP4200: Added support for Zynq 1 GHz.

- Encoder Out: A parameter is added for the Z pulse width. It sets the width of the Z pulse slice block under the mask. Encoder Output: New "Synchronization pulse width" added to the documentation. (FPGATT-64)

- Synthesis Manager block: enlarged the FPGA Development board dialog box.

- Added support Vivado 2017.2 and Matlab 2016B and 2017A.

Bugfixes

- Made correction in the rtxsg_tools.slx for being visible in Simulink browser RT-XSG/Tools. (FPGATT-59)

- Fixed the error of emcclk when arrive write_bitstream process for OP4500 with Vivado 2016.3. (FPGATT-65)

- Fixed deadlock on TX_READY signal (TX_READY always stays at zero after a fifo full). (FPGATT-72)

Version 3.1.6

Features

- Added support of RS485 TypeB Mezzanine(OP5368) for the OP4510 and OP5707 systems.

- Vivado 2017.1 and Matlab R2016A support.

- OP5342 full support for OP4510 and OP4200, restricted support for OP5#07 (specific customer only).

- Added Hardware Configuration and Interconnections Generation (HCIG) algorithm's scripts and documentation. (GFDB-##)

- An opVerifyAuroraBlockparams.m is a new script for gathering all Generic Aurora Blocks in a model and proceed to a verification off these parameters: MGT Reset Input use, MGT reference clock (for same MGT Quad), MGT Line rate (or same MGT Quad). (RTXSG-40)

Bugfixes

- Fix the problem of incoherence in the selection of the FPGA between the Synthesis block and the Hardware Configuration block (RTXSG-37)

Version 3.1.5

Features

- Added a parallelizer and a serializer blocks. (FPGATT-51)

- OP5342 support for the OP5607 / OP5707 with 1 MSPS limitation: new timing constraints (slot's granularity).

- Update Synthesis Manager Block: Before setting the interface block parameters, the CarrierName parameter (from the HardwareConfig block) must be verified and updated if necessary.(FPGATT-34)

- New Synthesis Manager Block: merge Version, Hardware and Synthesis Blocks in the same block (SynthesisManager). This new feature automatically updates older models with the new block.

- Resynchronisation software: "Update Requests" generation support and overrun's notification (data transfer even if overrun).

- Update block "Register max fanout": was using efsDisplayCb from eFPGAsim, changed to xsgDisplayCb.

- Update IO Block GUI: Verify if IO blocks need to be updated/reconfigured after the hardware change in the Hardware Config Block.

Bugfixes

- Fixed an issue with the default IPCache and Partition values in the new SynthesisManager block

- Fixed an issue caused an error when checking the path oh the model

- Matlab R2015B support. Correction in opxsgGetBitstreamVersion.m. (RTXSG-29)

Improved Documentation and Error Reporting

- OPAL_RT_VivadoPathCheck for informing through a warning message that some characters in the Vivado temporary path could be harmful.

Version 3.1.4

Features

- Register-Correction of reading the Alpha ID in the RTXSG version and changing the encoding.

- MGT/SFP-Added a delay on o_SDA and on o_Z for respecting the I2C specification hold timing of 100 ns for the Si5338 clock generator (clock reference).

- OP5342-Added support of an analog input mezzanine "OP5342" @ maximum 2 MSPS (but maximum 1 MSPS for OP5#07).

- MATLAB Function-MCode function to serialize words to the Aurora AXI interface (soft/Simulink/libRxx/m/opxsgGenericAuroraSender.m).

Bugfixes

- Vivado and Windows 7-Apply a workaround to fix problem with 260 characters limitations for PATH in Windows. The problem occurs mostly when Sysgen is generating and synthesizing IP cores.

Improved Documentation and Error Reporting

- Error Management - Added function of reporting errors (with file location and line number information; soft/Simulink/libRxx/m/CatchErrorReporter.m).

Version 3.1.3

Features

- Vivado: Added support of Vivado 2015.4 by taking into account the Xilinx Compilation type "Synthesized_Checkpoint".

- OP4200: Added support of User LEDs.

- Vivado: Added support of 2016.3 (added synth_stub option in Tcl script for generating the user model stub) with IP Cache option available for better Synthesis time achievement.

- VC707: Updated the Gray Zone by adding dont_touch attribute on configuration clock for generating a bitstream.

- OP4200 and Vivado 2016.3: Changed a constraint for allowing the generation of a bitstream (SPIx1).

- Updated the Selectable DIO block (specific to the TSDIO functionality) by adding a delay before the Model Synchronization pulse. (TT#8978)

- Mezzanine OP5342: Added support of the new Analog IN at 2 MSPS for OP4510 and OP5607 with Signal Integrity control (IO's drive strength specific modifications; additional timing constraints).

- Mezzanine OP5342: Bring correction on safe frequency support of the I2C communication bus under the user clock following (100 or 200 MHz).

- Selectable DIO: added synchronization on ModelSync for Selectable DO (rtxsg_application_lib.slx).

Bugfixes

- OP4510: Fixed issue with Expansion slot IO Block configuration (ExpansionSignal type). (TT#8969)

Improved Documentation and Error Reporting

- Added new report as hardware configuration file (Product, FPGA, mezzanine names) in the project folder (hw_config.txt).

Version 3.1.2

Features

- Add an option to enable or disable the CRC in the Generic Aurora. (TT#8951)

- Added support for new IO carrier names of the OP4200 system. (TT#)

- Added feature to generate the update request internally for OP4500. (TT8937#)

Bugfixes

- Fixed One step delay in Generic Aurora transmission when one word is transmitted per time step. (TT#8839)

- Fixed fatal exception again Matlab 2015aSP1. (TT8888#)

- Modify design to prevent flipping board index problem on OP4510 system. (TT8938#)

Version 3.1.1

Features

- Added mask for XSG blackbox resynch_fanout10_ff (register with MAX_FANOUT) attribute. The existing way to instantiate this blackbox manually in the designs has the disadvantage that the value of the MAX_FANOUT attribute is the same across all instances of this blackbox.By using this mask the value of the attribute can be changed with a mask parameter. (TT#8556)

- Added support for Board Index > 31 for the OP5607 (VC707). (TT#8748)

Bugfixes

- Fixed Mask Visibility of PWMO block When option "As Block Parameter" is chosen for InitPhase. (TT#8829)

Version 3.1.0

Features

- Added a "Selectable DIO" functionnality in RT-XSG. (TT#8791)

- Added support for Matlab 2015aSP1. (TT#8607)

- Added support for OP4200 (Zynq 7030) (alpha release). (TT#8741)

- Added support for OP5363 mezzanine (32 DI High Impedance) for Virtex-7 (OP5700, OP5607), and Kintex-7 (OP4510,OP4520). (TT#8369)

- Added a mechanism to detect a model crash in Hypersim, so that a protection logic can be implemented for the outputs of the simulator. (TT#8739)

- Added a protection to prevent endless error reporting when performing an update diagram (Ctrl-D) on a model when the Version block name is not exactly 'Version'. (TT#8757)

- Replaced the feature "open timing analyzer" by a timing text-file report. (TT#8623)

Bugfixes

- Fixed SineCosine block obsolescence in Common/op_cosin block with interpolated-LUT-based sine wave generator. (TT#4472)

- Fixed Park/Inversed Park transform blocks with updated Common/op_cosin block. (TT#8576, RT3#284360)

- Fixed an issue preventing the support of space characters in the model path. (TT#8622)

- Fixed an issue causing timing violation errors when generating bitstreams for OP4500. (TT#8783)

- Fixed an issue with chassis ID value changing from 0 to 31 after bitstream is programmed on systems with Virtex7 FPGA. (TT#8793)

Version 3.0.0

Features

- Added an option in the Version block to force the maximum fanout value for the ModelSync and nRst signals. (TT#8556)

- Improved PCIe timing management for Kintex7 FPGA (MMPK7 and TE0741) by relaxing maxskew parameter. (TT#8503)

Bugfixes

- Fixed filtering of input signals for TSDI and PWMI operating at 200MHz. (TT#8573)

- Fixed Generic Aurora Communication block to prevent Matlab crash at model opening. (TT#8505)

RT-XSG for ISE

Version 2.3.7

Features

- MMC synthesized netlists support

- Quadrature/Rotary encoder upgrade

- New Serializer/parallelizer library

Bugfixes

- Fixed LED blincking Synchronization across OP6000's TD-PCIe cards

- Aurora fix on signal TX_READY

Version 2.3.6

Features

- Support TestDrive in PCIe mode (OP6000-NxtGen, soft/extra_examples/TD_PCIe).

- Added synchronization on ModelSync for Selectable DO (Static branch) signals as the DataIn port should be asynchronous. Model Synchronization pulse converted to boolean. (RT3#297145).

- Add feature to generate the update request internally inside the FPGA. The default mode is as of now that is the update request is sent by the driver. The new mode is activated by setting a bit to 1 inside the FPGA's register. (TT#8937)

Bugfixes

- Fixing a mistake related to committing the same Lib file for both ISE and Vivado. Manually added the delay to the SDI block. Fixed a bug with the Selectable DIO block. The bug was specific to the TSDI O functionality which did not work for all frequencies and\or duty cycles. The fix was to add a delay before the Model Sync in the DOSelectable0 block.

- Resolve timing violation on reset signal in VC707 gray zone.

- Fix issue when datawidth is set to 32 and beyond in spi_loopback_on_op5236 RT-LAB and RT-XSG models.

- Fix flipping board index with using a 126-0506 interface board (OP4510, OP5600/ML605).

- Fixed error in block "Rescale to Fixed-Pt format" for removing any inconvenient "The current threshold values are being ognored". (TT #8881)

Version 2.3.5

Features

- Added an option in the Version block to force the maximum fanout value for the ModelSync and nRst signals.(TT#8556)

- Added Selectable DIO functionality with examples. (TT#8791)

- Integration of the OP5332's support with important corrections in the io_block.m. Only the Spartan3 has 2 synthesized netlists: 1 MSPS and 2 MSPS whereas the Virtex6 has only 2 MSPS one. (TT#8820)

Bugfixes

- PWM Out - Fix Mask visibility of the InitPhase when "As Block Parameter" is chosen (is not hidden). (TT#8829, RT3 #291538)

Version 2.3.4

Features

- Added a mechanism to detect a model crash in Hypersim, so that a protection logic can be implemented for the outputs of the simulator. (TT#)

- Added support for OP5332 mezzanine (16 analog Outputs, 2MS/s, pair isolated) on OP5600 (OP5142 and ML605). (TT#8740)

- Added a "Selectable DIO" functionnality in RT-XSG. (TT#8791)

- Added support for OP5363 mezzanine (32DIn High Impedance) for OP5600 (Spartan3 and Virtex6). (TT#8792)

Bugfixes

- Fixed an issue with chassis ID value changing from 0 to 31 after bitstream is programmed on systems with Virtex7 FPGA. (TT#8793)

- Fixed SineCosine block error in example model Sinusoidal_AnalogIO_rtxsg.mdl for OP5142. (TT#8797)

- Fixed an issue with the quadrature encoder input speed measurement observed when the QEI Packing block was not directly connected to the DataOUT block. (TT#8837)

Version 2.3.3

Bugfixes

- Fixed SineCosine block obsolescence in Common/op_cosin block with interpolated-LUT-based sine wave generator. (TT#4472)

- Fixed Park/Inversed Park transform blocks with updated Common/op_cosin block. (TT#8576, RT3#284360)

Version 2.3.2

Features

- Added an option in the Version block to force the maximum fanout value for the ModelSync and nRst signals. (TT#8556)

- Improved PCIe timing management for Kintex7 FPGA (MMPK7 and TE0741) by relaxing maxskew parameter. (TT#8503)

- Added support for the OP5963 optical-fiber synchronization card. It is compatible with OP5142 and ML605_2. (TT#8572)

Bugfixes

- Fixed filtering of input signals for TSDI and PWMI operating at 200MHz. (TT#8573)

- Fixed Generic Aurora Communication block to prevent Matlab crash at model opening. (TT#8505)

Version 2.3.1

Features

- Added support for SPI communication on OP5600/ML605 systems. (TT#8516)

Bugfixes

- Fixed an issue with the Pulse-Width Modulated Input (PWMI) block introduced in RT-XSG v2.3.0, causing the measured frequency and duty ratio to remain fixed at their minimum value. (TT#8510)

Version 2.3.0

Features

- Improved Generic Aurora protocol for high speed optical fiber communication to prevent erroneous behaviour at start of simulation on Hypersim. (TT#8491)

- Added high-speed mode for OP5330 Analog Output interface. This enable sampling period down to 440 ns by using 8 of the 16 channels of the interface. (TT#8488)

- Added support for Trenz Kintex7 FPGA (160T, 325T and 410T) for use in O4510 chassis. Support includes all features needed in RT-LAB simulation like PCIe communication, flash programming, control of the 4 I/O mezzanine modules, expansion I/O module (RS422 or optical fiber) and User LEDs, support of the SFP ports. (TT#8437)

- Updated Orion communication protocol to add support for variable number of words in messages, and a command header word. (TT#8403)

- Improved Orion protocol stability for communication between OP7000 and OP4510. (TT#8400)

- The PWMO block is now synchronized with the model, preventing drifting between identically configured pulse-width modulated signals generated simultaneously on different chassis. (TT#8326, RT3#276464)

Bugfixes

- Fixed Orion protocol to support 100MHz clock frequency on OP7000 systems. (TT#8399)

- Fixed an issue with PWMI function where the outputs would keep their values until the input signal switches. When the PWM is static (duty = 100% / 0%), the period is now

forced to the maximum value, and the time on to the maximum or minimum value depending if the state of the DIN is High or Low. (TT#7849)

Version 2.2.6

Features

- Added support for the 32DIn high impedance mezzanine (126-0515) on the OP5600/OP5142 platform. (TT#8320)

- Limit options for the OP4500 hardware configuration in the opxsgHardConfigGUI dialog. The OP4500 has two permanently integrated digital IO cards on the Slot#1 Section A (digital IN) and B (digital OUT). (TT#8276)

Version 2.2.5

Features

- Added 2 Gpbs data rate capability to the Inter-FPGA communication block. (TT#8245)

Version 2.2.4

Features

- Add support for the new interface card 126-0506 with the OP5600 variant of the ML605. The software remains compatible with older bitstreams and hardware, while the new firmwares are compatible with all hardware generations. (TT#7965)

Bugfixes

- Correction within the DAC controller to eliminate the risk that the reset signal could cause a hold time violation. (TT#8141)

Version 2.2.3

Features

- Added support for the new level-shifter board for ML605 (126-0506). (TT#7965)

- Added support for Analog In 8 Channel (126-0513 OP5340-2) (TT#8110)

- Added support for fallback for VC707 and MMPK7. (TT#8107)

- QEO and Resolver Unpacking blocks now support the StartOfFrame signal to be aligned with the data. (TT#8106)

- Enhanced OP5340 (Analog input card) interface to facilitate timing requirement closure during bitstream generation. (TT#8096, RT3#274455)

- Added support for ORION protocol. (TT#8072)

- Added support for Kintex7 card MMPK7-410T. (TT#8062)

Bugfixes

- Fixed an issue with the DataIN protection logic circuit when transitioning from execute to pause and back to execute state. (TT#8109)

Improved Documentation and Error Reporting

- Updated documentation for the InterFPGA SFP comm block in order to reflect recent changes and the correct block usage. (TT#8108)

Deprecation and Removals

- Removed the opUpdateDiagram function from the product (the file name conflicted with the RT-LAB toolbox). (TT#8024)

Version 2.2.2

Features

- Added support for InterFPGA communication on VC707 OP7020/OP5607 Systems (Inter-FPGA et MMC communication Block have been reworked for V6, V7, K7). (TT#8036)

- Added support for 16-bit bitstream_minorid (was 5-bit). (TT#8035)

- TSDI block: Enabled the edge type selection parameter detected to be selected from an input port (TT#8033)

- Added Differential I/O block (a.k.a Encoder) for OP4500 system. (TT#7844)

- Added the Resolver In/Out Examples for OP7161/ML605/OP4500. (TT#7369)

Bugfixes

- Fixed an issue related to OP7000 inter-FPGA commincation blocks causing Matlab to crash during bitstream generation or offline simulation of the RT-XSG model. (TT#7958)

- Fixed an issue with DataIn unpacking blocks related to signals dropping to zero when simulation overruns occur. (TT#7933)

Deprecation and Removals

- Dropped support for OP5130 (Virtex2P), ML505, ML506 (XSG and standalone), ML507, and Xilinx/Digilent XUPV5-lx110T FPGA cards (obsolete). (TT#8034)

Version 2.2.1

Features

- Added support for Opal-RT OP5360-1 Digital Mezzanine Push-Pull FET 5 to 15V, 50ns - 32 Dout. (TT#8037)

- Added support for OP4500 Kintex7-based hardware platform (alpha). (TT#7844)

- Added support for use of Din in the back of the OP7162 secondary FPGA. (TT#7786)

- Added analog and digital I/O support for VC707-based hardware platforms (OP5607 chassis). (TT#7741)

- Added support for OP7824 - 16 Channels Dout Fiber Optic card. (TT#7727)

- Updated the XSG Aurora block to output statistics on the data traffic going through the block (TX error, RX error, overflows, etc.). (TT#7714)

- Updated Resolver In Packing block. Updated the OP5142 Resolver In/Out example model. (TT#7369)

Bugfixes

- Fixed various issues related to the copy of report files: Matlab diary is created in RT-XSG directory, fpga_model_sysgen_error.log is transfered, the CDC file is transfered, the MRP file is transfered if a MAP error is detected. (TT#7967)

- Fixed an issue with ML605 firmwares that resulted in the RT-LAB model execution giving a "Timeout waiting for valid bit" error during model execution. (TT#7813, RT3#271671)

- Fixed an issue with the TSDO block in which the events might be delayed by one simulation step. (TT#7790)

- Fixed a crash that was happening when generating a bitstream with more than 4 SFP on the OP7020. (TT#7746)

Version 2.2.0

Features

- Added support for the 35mA Analog Out mezzanine in OP5600 target. (TT#7165)

Version 2.1.6a

Features

- Added 200MHz support for OP5341 (Fast AIN 2MS). (TT#7129)

- Resolver Out: Added amplitudes for SinResolver and CosResolver independant from carrier amplitude. (TT#7111, RT3#264678)

Bugfixes

- OP7000: fixed synchronization issue between OP7000 chassis (sporadic overruns). (TT#7325)

- Fixed issues with the resolver out block. Amplitude for sinus and cosinus are selected independently from carrier amplitude. (TT#7111, RT3#264678)

Version 2.1.7

Bugfixes

- Fix crash of MatLab when installing RT-XSG on Windows XP. (TT#7370)

Version 2.1.5

Bugfixes

- Fixed issue while using A/D channels at 200 MHz. (TT#7268, RT3#266105)

Version 2.1.3

Bugfixes

- Fixed problem of OP5330 Load_DAC command duplication for one buffer. (TT#6962, RT3#262970)

- Fixed problem of contention, overheat on mezzanine and FPGA when DIN/AIN mezzanine is physically present when loading a bitstream where this I/O slot/group is unused. (TT#6755, RT3#263151)

Version 2.1.2

Bugfixes

- Fixed issue with PWM Out block. Duty of the signal suddenly dropped to 0. (TT#6889, RT3#262656)

Improved Documentation and Error Reporting

- Clarified the specifications of the TSDout RT-XSG block. The minimal delay between two pulses is 40 ns. The documentation is up-to-date. (TT#6799, RT3#260778)

Version 2.1.1

Features

- Added a new XSG Scope. This scope can monitor up to 32 channels with:
- Up to 250 samples per CPU model time step
- User-friendly graphical interface
- Data resolution selection (16 bits or free)
This RT-XSG block is associated to an RT-LAB block. (TT#6785)

Bugfixes

- Fixed calibration model for Analog In block. (TT#6848)

- Fixed problem when generating events shortly before the end of the model time step (40 ns) using TSDO. (TT#6812)

- Fixed problem with Resolver Out when using external carrier (wrong amplitude). (TT#6747, RT3#261629)

- Fixed crash at compilation under Windows 7 (64 bits). (TT#6680)

Version 2.1.0

Features

- Modification of Resolver In block output order:
    pin1 CarrierOut
    pin2 Theta
    pin3 RotorfreqBase
    pin4 Error

Modification of ResolverIn packing input order:
    pin1 Sync
    pin2 Theta1
    pin3 RotorFreqBase1
    pin4 Theta2
    pin5 RotorFreqBase2 (TT#6656)

- Update of the Hardware Config XSG block documentation. (TT#6636)

- Added new SPI block. (TT#6272, RT3#223779)

- Added support for PCIe Xilink patch. THIS PATCH IS REQUIRED in order to be able to generate bitstream with RT-XSG. (TT#6574)

- Added support for ML605 I/O. (TT#6355)

- Increased the Maximum Frequency of the PWM output block to 200Mhz. (TT#6511)

- Added support for I/O on BP1 connector. (TT#6507)

- Added new ResolverIn and ResolverOut block. (TT#6474)

- Added support for DDR3 memory controller. (TT#6340)

- Added support for ML605. (TT#6295)

- Added support for differential mode, resolution and direction in Quad encoder block. (TT#5251)

- Added support for OP5237-3 Isolated High Voltage 16-Pull-16-Push Hybrid 32out/30in Digital Interface (TT#6415)

- Added support for multiple ranges for the calibration. (TT#6398)

- Added support to execute XSG at 200Mhz on ML605. (TT#6338)

- Added support for MATLAB R2010a and R2010b. (TT#6262)

- Added the Floating-Point FPGA State-Space solver. (TT#5897)

- Added 4 example models for the ML605:
1- Simple Multiply and Add
2- PWM and Digital I/O
3- Analog In/Out
4- DIO, TSDIO, QEIO, AIO (TT#6635, RT3#260904)

- Added a new configuration parameter of Encoder In: resolution. (TT#6539, RT3#258775)

Bugfixes

- Fixed FPGA drive output to fix problem with Analog In board. (TT#6579, RT3#260422)

- Fixed bug when selecting OP5236-1 board in Hardware Config block. (TT#6651)

- Fixed problem with OP5142 XSG bitbasher block (wrong endianness). (TT#6551, RT3#258775)

- Fixed DDR3 issues with ML605. (TT#6571)

- Fixed PWMO unpacking block. (TT#6562)

- Fixed support for new DIN Mezzanine. Added a new ID board. (TT#6558)

- Fixed incorrect number for digital I/O board. (TT#6553)

- Fixed Analog Out block that was keeping the last value after reset. (TT#6487, RT3#258403)

- Fixed TSDIn block to send an initial state when no event has been detected. (TT#6327)

- Fixed "-k" option that is not supported with xilink 12.1. (TT#6107)

- Fixed TSBIn block to remove an additional delay. (TT#6091)

Improved Documentation and Error Reporting

- Update of the Resolver In block documentation. (TT#6654)