
# OP6221 Base Module
# User Guide

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# BASE MODULE

## INTRODUCTION

This document contains sections pertaining to the installation, architecture and features of the Base module.

All simulators have a Base module, which contains a digital controller that drives the simulator chassis. It also contains the power moding circuitry that drives the power bus.

The board has the following capabilities:

- Monitoring of the operating power supply (simulator power) provided to all modules
- Control of the power moding circuitry which resides on the power backplane and drives the power bus
- A serial interface, provided to analyze the connection of serial tools to the ECU.

The board provides the following benefits:

- Cable and harness identification
- Module identification and listing
- On site firmware updates
- Trigger output based on engine position for easy logic analyzer and oscilloscope capture of high speed transient

## ARCHITECTURE OVERVIEW

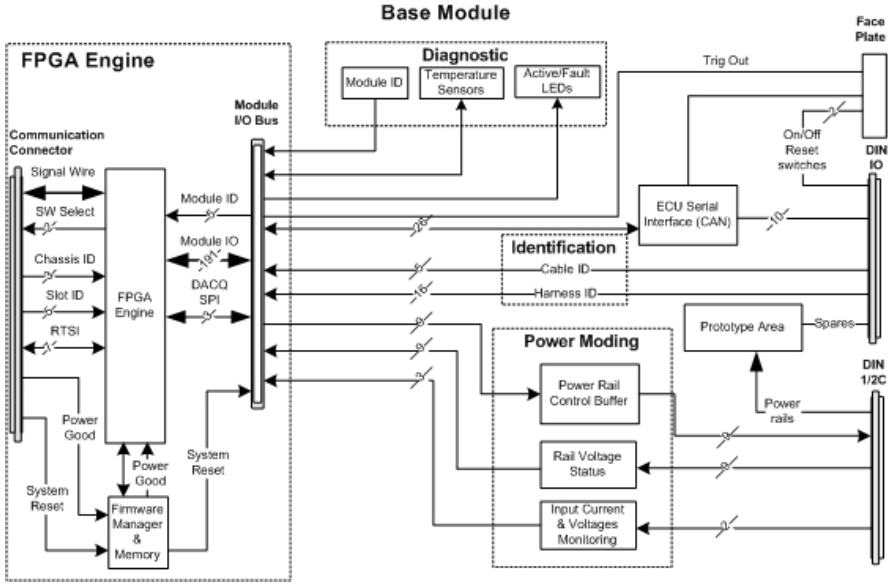



Figure 8: Base Module block diagram with the FPGA engine

The “Base Module Firmware Block Diagram” shows the block diagram of the Base module’s embedded firmware. The firmware is mainly composed of the following elements:

- Communication Bus Interface
- Battery Control Module
- Key Switch Module
- Rail Control Module
- CAN Termination
- Serial Line (State & Transition Counters)
- Synchronization Unit
- Position Synchronization Module

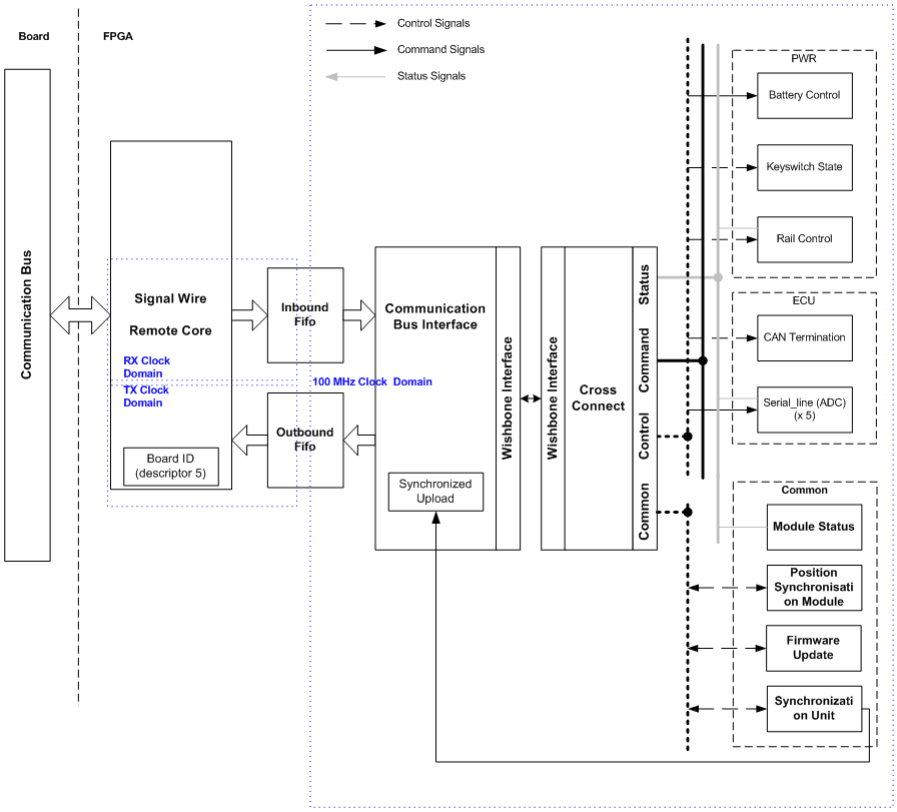



Figure 9: Base Module Firmware Block Diagram

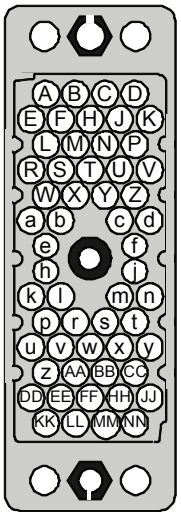
# BOARD FEATURES

## I/O Connections

The I/O signals table lists the signals available on the external connector and on the system's backplane.

| Elco Eq. # (female) | Elco Pin name (female) | Signal Name in Analog Module Schematic (2003/10/07) | Input Line | Output Line | Refe-rence | DIN 96/J7A |
|---|---|---|---|---|---|---|
| 1 | A | OUT_A0 | | x | 2.x.2 | A2 |
| 2 | B | REF_L2 | x | | 2.x.3 | C1 |
| 3 | C | REF_L0 | x | | 2.x.3 | B1 |
| 4 | D | REF_H0 | | | 2.x.1 | A1 |
| 5 | E | REF_L4 | x | | 2.x.3 | C3 |
| 6 | F | REF_H1 | x | | 2.x.1 | B3 |
| 7 | H | OUT_A1 | | x | 2.x.2 | A3 |
| 8 | J | PROTO0 | x | x | 2.x.5 | C2 |
| 9 | K | PROTO1 | x | x | 2.x.5 | B2 |
| 10 | L | OUT_A3 | | x | 2.x.2 | A5 |
| 11 | M | REF_L5 | x | | 2.x.3 | C4 |
| 12 | N | REF_H2 | x | | 2.x.1 | B4 |
| 13 | P | OUT_A2 | | x | 2.x.2 | A4 |
| 14 | R | REF_L7 | x | | 2.x.3 | C6 |
| 15 | S | REF_H4 | x | | 2.x.1 | B6 |
| 16 | T | OUT_A4 | | x | 2.x.2 | A6 |
| 17 | U | REF_L6 | x | | 2.x.3 | C5 |
| 18 | V | REF_H3 | x | | 2.x.1 | B5 |
| 19 | W | OUT_A6 | | x | 2.x.2 | A8 |
| 20 | X | REF_L8 | x | | 2.x.3 | C7 |
| 21 | Y | REF_H5 | x | | 2.x.1 | B7 |
| 22 | Z | OUT_A5 | | x | 2.x.2 | A7 |
| 23 | a | REF_H7 | x | | 2.x.1 | B9 |
| 24 | b | OUT_A7 | | x | 2.x.2 | A9 |
| 25 | c | REF_L9 | x | | 2.x.3 | C8 |
| 26 | d | REF_H6 | x | | 2.x.1 | B8 |
| 27 | e | OUT_A8 | | x | 2.x.2 | A10 |
| 28 | f | REF_L10 | x | | 2.x.3 | C9 |
| 29 | h | REF_L11 | x | | 2.x.3 | C10 |
| 30 | j | REF_H8 | x | | 2.x.1 | B10 |
| 31 | k | OUT_A10 | | x | 2.x.2 | A12 |
| 32 | l | REF_L12 | x | | 2.x.3 | C11 |
| 33 | m | REF_H9 | x | | 2.x.1 | B11 |
| 34 | n | OUT_A9 | | x | 2.x.2 | A11 |
| 35 | p | REF_H11 | x | | 2.x.1 | B13 |
| 36 | r | OUT_A11 | | x | 2.x.2 | A13 |
| 37 | s | REF_L13 | x | | 2.x.3 | C12 |
| 38 | t | REF_H10 | x | | 2.x.1 | B12 |
| 39 | u | OUT_A13 | | x | 2.x.2 | A15 |
| 40 | v | REF_L15 | x | | 2.x.3 | C14 |
| 41 | w | REF_H12 | x | | 2.x.1 | B14 |
| 42 | x | OUT_A12 | | x | 2.x.2 | A14 |
| 43 | y | REF_L14 | x | | 2.x.3 | C13 |
| 44 | z | REF_H14 | x | | 2.x.1 | B16 |
| 45 | AA | OUT_A14 | | x | 2.x.2 | A16 |
| 46 | BB | REF_L1 | x | | 2.x.3 | C15 |
| 47 | CC | REF_H13 | x | | 2.x.1 | B15 |
| 48 | DD | ID_CBL0 | x | | 2.x.4 | A18 |

Female
ELCO Connector
56 pins



| Elco Eq. # (female) | Elco Pin name (female) | Signal Name in Analog Module Schematic (2003/10/07) | Input Line | Output Line | Refe-rence | DIN 96/J7A |
|---|---|---|---|---|---|---|
| 49 | EE | ID_CBL | | x | 2.x.4 | C17 |
| 50 | FF | REF_H15 | x | | 2.x.1 | B17 |
| 51 | HH | OUT_A15 | | x | 2.x.2 | A17 |
| 52 | JJ | REF_L3 | x | | 2.x.3 | C16 |
| 53 | KK | ID_CBL4 | x | | 2.x.4 | C20 |
| 54 | LL | ID_CBL3 | x | | 2.x.4 | C19 |
| 55 | MM | ID_CBL2 | x | | 2.x.4 | A19 |
| 56 | NN | ID_CBL1 | x | | 2.x.4 | C18 |
| Note: Artwork was done using Elco Male and female connector was used during assembly | | | | | | |

Table 4: Base Module DIN I/O Signal Description

## MODULE LEDS

Each module's state is displayed using 3 LEDs:

| LED | Indicator | Description |
|---|---|---|
| Green | Power | Indicates that the digital power supply for 5 V or 3.3V are within the validity range. This LED is not software controlled |
| Yellow | Activity | Driven by the FPGA. This LED indicates that the FPGA has been configured and the communication has been reset by the real-time unit (RTU). This LED shows that the FPGA engine of the module is able to communicate with the RTU<br>The yellow LED indicates error codes when the RED led is ON:<br>• No blink: general error<br>• 2 blinks: the FPGA module is not programmed, you need to perform flash update operation.<br>• 3 blinks: the FPGA firmware does not correspond to current module. (e.g. The FPGA is programmed for a Base Module but is inserted on Switch Module.) |
| Red | Fault | Driven by the FPGA. This LED indicates that a fault has been detected in the system. These faults are, but are not limited to: over tension, over current and software fault. Other software faults are raised under the following conditions:<br>• Invalid configuration, e.g. Enabling several power rails for an output signal<br>• Invalid output driver selection<br>• Invalid model conditions |

The FPGA prevents invalid configuration, however, it lets the fault LEDs inform the operator of an abnormal condition. In addition, the error is reported to the model.

# SYSTEM IDENTIFICATION

## Cable Identification (ID_CBL5-0)

These five input signals are used by the real-time unit to identify which harness connector is attached to the module. Each of these signals is pulled up to 5V through a 100 kΩ resistor. When the harness connector is plugged into the simulator it grounds the selected signals to provide the simulator with the cable ID (see “Cable Identification”). For example, if the first and fourth signals (ID 0 and ID3) are shorted to the ground, the simulator returns 22 (10110) for the cable ID.

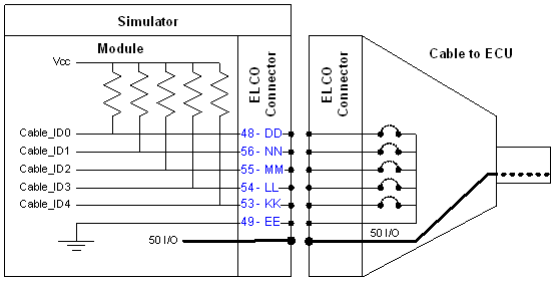



Figure 10: Cable Identification

## Harness Identification (ID_HRNS15-0)

16 harness ID signals are provided. Each of these signals is pulled up to 5V through a 100 kΩ minimum, resistor. Harness ID is determined by the grounded signals as explained in the previous sub-section Cable Identification and is illustrated in Figure 10.

# ECU SERIAL INTERFACE

This feature provides you with a front panel interface between the ECU and a diagnostic scan tool. Signals are routed from the harness to the front panel. These signals are hooked to female banana jack (Figure 13) and D-Shell 9 Pin Connectors. as shown in the following tables. You are able to monitor the activity on the signals shown in Table 5. The inputs are operating voltage tolerant and have an input impedance greater than 100 kΩ. The state of the input is monitored over a one second window sampled at 1 kHz. All voltages listed are derived from the harness connector.

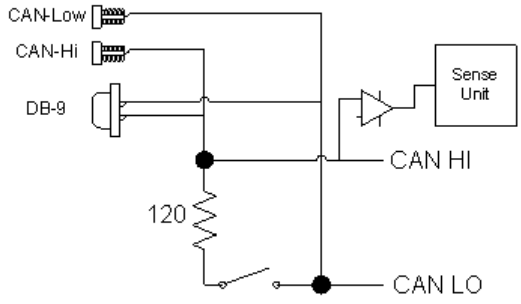



Figure 11: CAN Monitor / Termination

For the K-Line, CAN 1- HI, CAN 2-HI and LS CAN input lines, the sense unit indicates a high when the input voltage is above 3.0 V and a low when the input is below 2.8 V. For the J1850, the sense unit indicates a high when the input voltage is above 4.1 V and a low when the input is below 3.8 V. The sense unit provides the simulator with three values: the digital current state, the analog current state and the transition count.

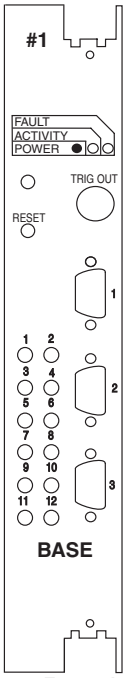



Figure 12: Front Panel of the Base Module

| Item | Signal |
|---|---|
| 1 | Primary J1850 |
| 2 | K-line |
| 3 | CAN1-High |
| 4 | CAN2-High |
| 5 | LS-CAN |

Table 5: Monitored Serial Signals

| Jack Number | Signal |
|---|---|
| 1 | Primary J1850 |
| 2 | Secondary J1850 (Ground) |
| 3 | +12 V |
| 4 | K-line |
| 5 | +12 V |
| 6 | Ground |
| 7 | CAN1-Low |
| 8 | CAN1-High |
| 9 | CAN2-Low |
| 10 | CAN2-High |
| 11 | LS-CAN |
| 12 | Ground |

Table 6: Serial Signals to Banana Jacks

## Serial Interface D-Shell 9 Pin Connectors

The signals shown in Table 7 are routed from the harness connector to D-Shell 9 Pin Connectors mounted on the front panel of the Base module.

| DB9 Connector # | Signal | DB9 Pin | ELCO 56 |
|---|---|---|---|
| 1 | CAN1-Low | 2 | B |
| | CAN1-High | 7 | C |
| 2 | CAN2-Low | 2 | E |
| | CAN2-High | 7 | J |
| 3 | LS-CAN | 2 | M |
| | Ground | 7 | h |

Table 7: Serial Signal List 9 Pin D

## CAN Termination

You can activate a termination resistor (120 O) between each pair of CAN signals (CAN X HI and CAN X LO.) LS CAN termination resistor is between LS CAN and ground and it has a value of 2.2 kΩ.

## Serial Line Module (ADC Controller)

The serial line module monitors serial lines. It also controls analog to digital converters to store the state of the analog line in a status register.

# POWER MODING

Power moding takes the battery input and creates moded power that is output through the power bus and routed to the output banana-jacks at the back of the chassis (see Figure 13). The Battery Input is protected with a 25 A fuse and each of the moded power output operates up to 25 A. The power backplane is designed with low resistance between the battery input and any of the moded power outputs featuring less than 25 mΩ.

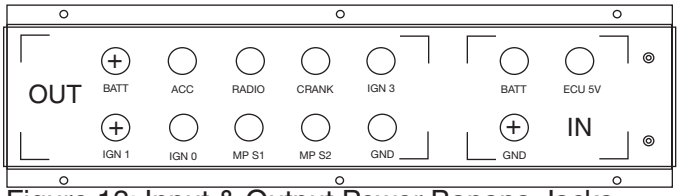



Figure 13: Input & Output Power Banana Jacks

The state of the power moded outputs is controlled as shown in Table 8. For each mode, each output set to HI is shorted to the battery input or opened when set to LO.

There are eight power modes. The power moding states are completely programmable. In addition to the shown moding, the state of a particular rail is controlled by the rail enable input.

The moded outputs are gated by the rail enable input. Any changes made to the rail enable input is immediately reflected in the state of the power moding outputs. See the “Rail Enable (Din_Rail_En_Inp)” section for more details.

| Mode | Moded Power Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **ACC** | **RADIO** | **CRANK** | **IGN3** | **IGN1** | **IGN0** | **UD1** | **UD2** |
| ACC | HI | HI | LO | LO | LO | LO | LO | LO |
| OFF/ LOCKED | LO | LO | LO | LO | LO | LO | LO | LO |
| UNLOCK | LO | LO | LO | LO | LO | HI | LO | LO |
| RUN | HI | HI | LO | HI | HI | HI | LO | LO |
| CRANK | LO | LO | HI | LO | LO | LO | LO | LO |
| OFF | LO | LO | LO | LO | LO | LO | LO | LO |
| SPARE 1 | LO | LO | LO | LO | LO | LO | LO | LO |
| SPARE2 | LO | LO | LO | LO | LO | LO | LO | LO |

Table 8: Power Moding

**NOTE:** when the battery line is disabled, all moded outputs are opened.

### Battery Control

You can control the state of the battery line. When the battery line is disabled, the connection between the battery input and the battery is opened (see Figure 8).

### Simulator Power

All module power is supplied by the internal power supply. The input power to the simulator is a standard 120 / 220 VAC 60/50 Hz input.

The simulator power is monitored. When it deviates from the acceptable operating range, an error is generated and the chassis protects itself and the ECU. This action could include, but is not limited to: dropping into an unconfigured state or shutting down until error circumstances have been corrected. The ground for all of the modules and the power ground used by the ECU are tied at a single point in the Base module.

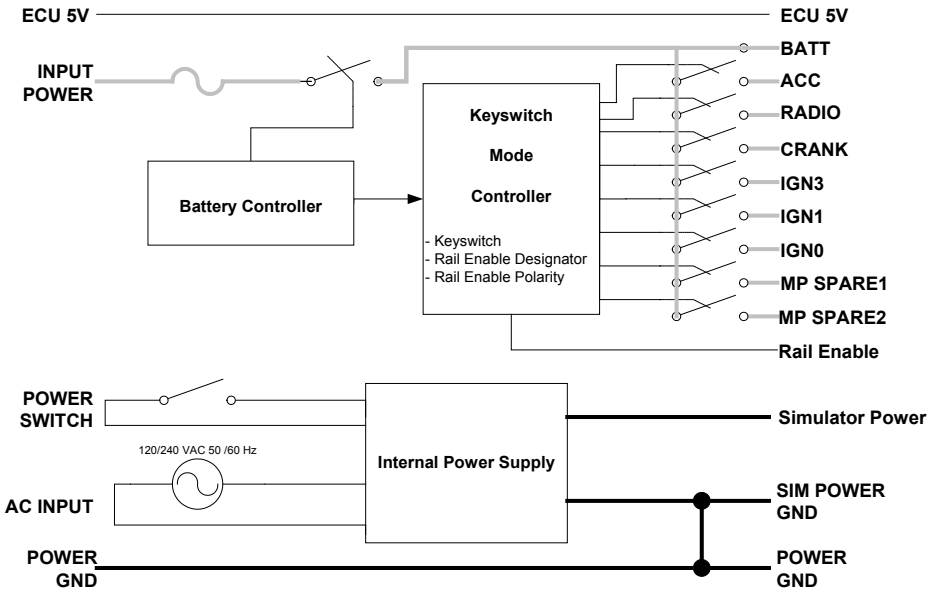



Figure 14: Power Moding Diagram

## BATTERY CONTROL

Battery control acts on the state of the battery line. A control register allows software to set the state of the output line. Also, a status register monitors the current state of the battery line.

## RAIL CONTROL

Rail control acts on the rail enable signal. It allows you to disable all the lines or to disable each line individually. Two control registers are used to set the active state of the rail enable signal and to determine the state of each line.

## KEY SWITCH STATE

Key Switch State controls the state of the power moding circuitry. A control register allows software to set the state of the output lines. Also, a status register monitors the current state of the power moding circuitry. Each line can be disabled individually according to the rail_mask input.

### Rail Enable (Din_Rail_En_Inp)

This high impedance input (>100 kΩ) is used to control the state of the power rail selected by the rail enable designator. The active state of this input is determined by the Rail Enable Polarity variable. The state of this signal is based on a 3.5 threshold voltage with hysteresis. When the input is above the threshold voltage, it is considered high. When the input voltage is below the threshold voltage, it is considered low. The appropriate bias voltage is applied to the input, by the simulator, to prevent accidental assertion of the power rail.

## TRIGGER OUT

This feature outputs a synchronization signal on the Base module BNC that is available on the front panel in order to synchronize a capture device such as an oscilloscope or a logic analyzer.

It can generate a trigger lasting 200 ns based on either the model synchronization, the high resolution signal or a trigger when the engine position reaches a specified value.

## SYNCHRONIZATION

A synchronization pulse that corresponds to the start of a calculation step is generated to enable synchronization between the different modules of the chassis. Because many operations are time related, this pulse is used to latch data (preserve the contents of the previous calculation step) and to reset registers and/or counters for the next time interval.

## FIRMWARE UPDATE

TestDrive modules support a robust remote firmware update mechanism. This mechanism is capable of recovering from a failure to update FPGA configuration data due to uncontrolled circumstances such as a power failure. In order to recover from such an incident, the FPGA engine includes an FPGA Safe Configuration Data Flash memory device. This memory device holds a bootstrap application code that is common to all Opal-RT modules. These modules are minimal components of any Opal-RT IO controller application allowing a module to be reprogrammed while the model application is in pause.

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