OP6223 Pulse Driven Load Module
User Guide

www.opal-rt.com

PULSE DRIVEN LOAD MODULE

INTRODUCTION

The Pulse Driven Load module is designed to measure the frequency, duty cycle and analog state of pulses from an external source or the ECU. This module supports 3 types of inputs; standard, bipolar and flexible.

The board exhibits the following capabilities:

- 32 standard pulse driven load inputs
- 2 flexible pulse driven load inputs
- 5 flexible pulse driven load inputs The board provides the following benefits:
- Cable identification
- Module identification and listing
- On site firmware update

ARCHITECTURE OVERVIEW

“Pulse Driven Load Module Electronic Board Diagram” shows the block diagram of the Pulse Driven Load module with the FPGA engine.

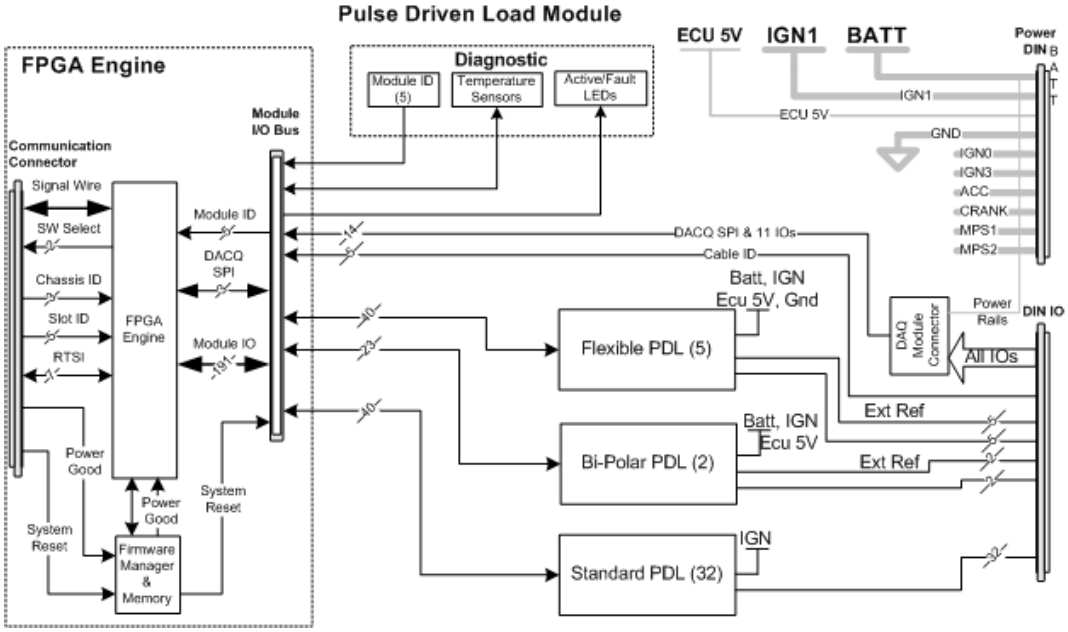


Figure 15: Pulse Driven Load Module Electronic Board Diagram

The firmware is mainly composed of the following elements:

- Standard PDL Unit
- Bipolar PDL Unit
- Power Rail Select Unit
- Communication Bus Interface
- Synchronization Unit

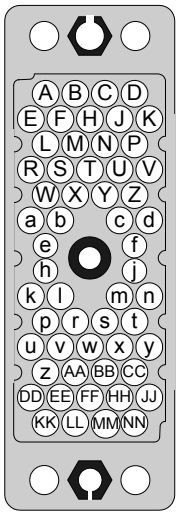
BOARD FEATURES

I/O Connections

Table 9 lists the signals available on the external connector and on the system's backplane.

Elco Eq. # (female)	Elco Pin name (female)	Signal Name in Analog Module Schematic (2003/10/07)	Input Line	Output Line	Refe-rence	DIN 96/J7A
1	A	OUT_A0		x	2.x.2	A2
2	B	REF_L2	x		2.x.3	C1
3	C	REF_L0	x		2.x.3	B1
4	D	REF_H0			2.x.1	A1
5	E	REF_L4	x		2.x.3	C3
6	F	REF_H1	x		2.x.1	B3
7	H	OUT_A1		x	2.x.2	A3
8	J	PROTO0	x	x	2.x.5	C2
9	K	PROTO1	x	x	2.x.5	B2
10	L	OUT_A3		x	2.x.2	A5
11	M	REF_L5	x		2.x.3	C4
12	N	REF_H2	x		2.x.1	B4
13	P	OUT_A2		x	2.x.2	A4
14	R	REF_L7	x		2.x.3	C6
15	S	REF_H4	x		2.x.1	B6
16	T	OUT_A4		x	2.x.2	A6
17	U	REF_L6	x		2.x.3	C5
18	V	REF_H3	x		2.x.1	B5
19	W	OUT_A6		x	2.x.2	A8
20	X	REF_L8	x		2.x.3	C7
21	Y	REF_H5	x		2.x.1	B7
22	Z	OUT_A5		x	2.x.2	A7
23	a	REF_H7	x		2.x.1	B9
24	b	OUT_A7		x	2.x.2	A9
25	c	REF_L9	x		2.x.3	C8
26	d	REF_H6	x		2.x.1	B8
27	e	OUT_A8		x	2.x.2	A10
28	f	REF_L10	x		2.x.3	C9
29	h	REF_L11	x		2.x.3	C10
30	j	REF_H8	x		2.x.1	B10
31	k	OUT_A10		x	2.x.2	A12
32	l	REF_L12	x		2.x.3	C11
33	m	REF_H9	x		2.x.1	B11
34	n	OUT_A9		x	2.x.2	A11
35	p	REF_H11	x		2.x.1	B13
36	r	OUT_A11		x	2.x.2	A13
37	s	REF_L13	x		2.x.3	C12
38	t	REF_H10	x		2.x.1	B12
39	u	OUT_A13		x	2.x.2	A15
40	v	REF_L15	x		2.x.3	C14
41	w	REF_H12	x		2.x.1	B14
42	x	OUT_A12		x	2.x.2	A14
43	y	REF_L14	x		2.x.3	C13
44	z	REF_H14	x		2.x.1	B16
45	AA	OUT_A14		x	2.x.2	A16
46	BB	REF_L1	x		2.x.3	C15
47	CC	REF_H13	x		2.x.1	B15
48	DD	ID_CBL0	x		2.x.4	A18
49	EE	ID_CBL		x	2.x.4	C17

Female
ELCO Connector
56 pins



Elco Eq. # (female)	Elco Pin name (female)	Signal Name in Analog Module Schematic (2003/10/07)	Input Line	Output Line	Refe-rence	DIN 96/J7A
50	FF	REF_H15	x		2.x.1	B17
51	HH	OUT_A15		x	2.x.2	A17
52	JJ	REF_L3	x		2.x.3	C16
53	KK	ID_CBL4	x		2.x.4	C20
54	LL	ID_CBL3	x		2.x.4	C19
55	MM	ID_CBL2	x		2.x.4	A19
56	NN	ID_CBL1	x		2.x.4	C18
Note: Artwork was done using Elco Male and female connector was used during assembly						

Table 9: Pulse Driven Load Module DIN I/O Signal Description

MODULE LEDS

Each module's state is displayed using 3 LEDs:

LED	Indicator	Description
Green	Power	Indicates that the digital power supply for 5 V or 3.3V are within the validity range. This LED is not software controlled
Yellow	Activity	Driven by the FPGA. Indicates that the FPGA has been configured and the communication has been reset by the real-time unit (RTU). This LED shows that the FPGA engine of the module is able to communicate with the RTU The yellow LED indicates error codes when the RED led is ON: • No blink: general error • 2 blinks: the FPGA module is not programmed, you must perform flash update operation. • 3 blinks: the FPGA firmware does not correspond to current module. (e.g. The FPGA is programmed for a Pulse Driven Load Module but is inserted on Switch Module.)
Red	Fault	Driven by the FPGA, the LED indicates that a fault has been detected in the system. These faults are, but not limited to: over tension, over current and software fault. Other software faults are raised under the following conditions: • Invalid configuration, e.g. Enabling several power rails for an output signal • Invalid output driver selection • Invalid model conditions

The FPGA prevents invalid configuration, however, it lets the fault LEDs inform the operator of an abnormal condition. In addition, the error is reported to the model.

SYSTEM IDENTIFICATION

Cable Identification (ID_CBL5-0)

These five input signals are used by the real-time unit to identify which harness connector is attached to the module. Each of these signals is pulled up to 5V through a 100 kΩ resistor. When the harness connector is plugged into the simulator it grounds the selected signals to provide the simulator with the cable ID (see Figure 3). For example, if the first and fourth signals (ID 0 and ID3) are shorted to the ground, the simulator returns 22 (10110) for the cable ID.

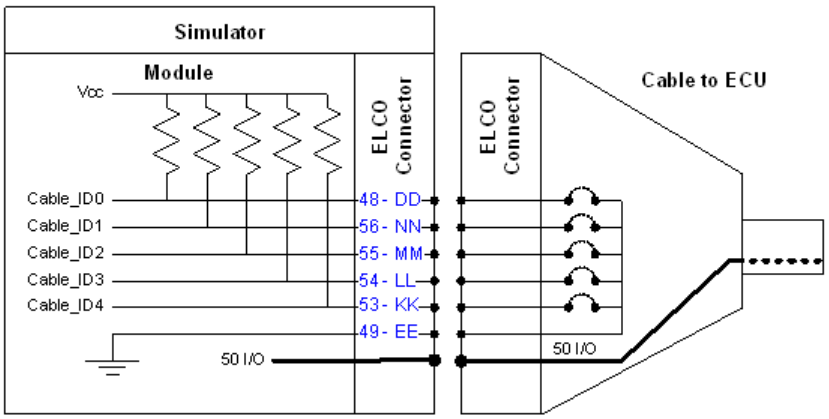


Figure 16: Cable Identification

PDL INPUTS

The PDL module has three types of inputs for monitoring signals: Standard, Bipolar and Flexible. The inputs' analog and digital states are continuously monitored to extract all transitions. Period and duty cycle is computed using the transition timestamps.

A 12 bits analog to digital converter is used to measure analog state. Each input's operating voltage is 0 to 16 V and the sense unit impedance is superior to 100K. All inputs are tolerant from –1 V to 27 V.

STANDARD PDL INPUTS

(STD_An, STD_Bn, STD_Cn, STD_Dn)

The 32 standard input lines are tied to either IGN1 or GND via a bias resistor. Standard PDL inputs are typically used to monitor digital signals with one of the following state combinations:

GND-IGN1(STD TYPE A,C,D) ; OPEN-IGN1(STD TYPE B); GND-OPEN (STD TYPE A,C,D)

The “Standard PDL Input Electrical Diagram” shows the electrical schematics of a standard PDL input. It illustrates that the input is internally connected to a specified rail voltage via bias resistor. Sense units indicate high when the input voltage is above 3.5 V ± 10% and low when the input is below 1.5 V ± 10%.

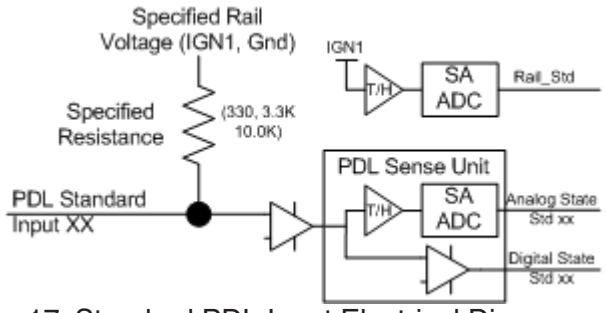


Figure 17: Standard PDL Input Electrical Diagram

The 32 standard PDL inputs are divided into four types defined below.

1. **Standard PDL Input - Type A (STD_A[16:0])**
   These 17 Standard PDL inputs have a 330 Ω tied to the IGN1 power rail**.**
2. **Standard PDL Input - Type B (STD_B[3:0])**
   These 4 Standard PDL inputs have a 330 Ω tied to GND.
3. **Standard PDL Input - Type C (STD_C[3:0])**
   These 4 Standard PDL inputs have a 3,3 kΩ tied to the IGN1 power rail.
4. **Standard PDL Input - Type D (STD_D[6:0])**
   These 7 Standard PDL inputs have a 10,0 kΩ tied to the IGN1 power rail.

BIPOLAR PDL INPUTS (BIP_[1:0] & B_EXTV[1:0])

The 2 bipolar inputs have configurable rail and a fixed bias set to 50% to rail voltage. Bipolar PDL inputs are typically used to monitor bipolar signals with a positive voltage offset.

Figure 18 shows that the input is internally connected to 50% of the rail voltage via bias resistors. Sense units indicate high when the input voltage is above 80% of rail voltage and low when the input is below 20% of rail voltage.

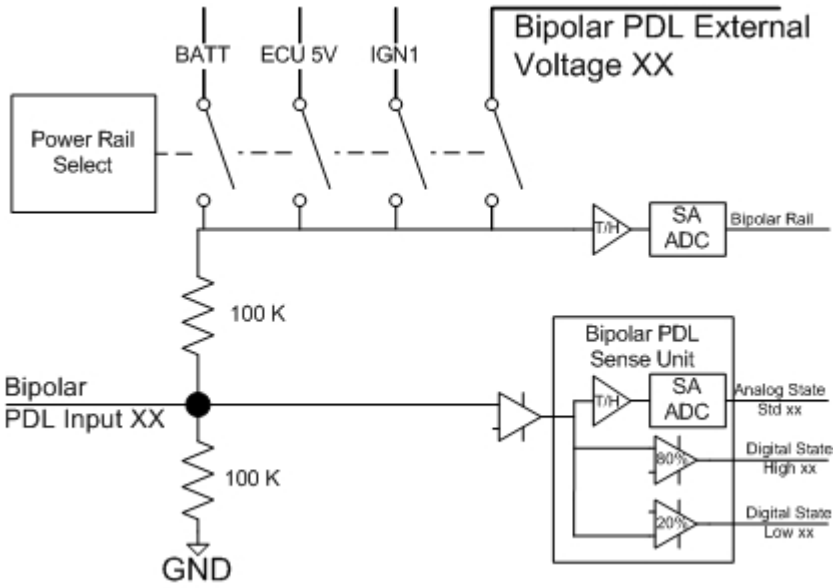


Figure 18: Bipolar PDL Input Electrical Diagram

FLEXIBLE PDL INPUTS (F_[4:0] & F_EXTV[4:0])

The 5 flexible inputs have configurable rail. Inputs are tied to rail via a bias resistor. Flexible PDL inputs are typically used to monitor digital signals that are referenced to **BATT**, **ECU5V**, **IGN1** or external voltage.

Figure 19 illustrates that the input is internally connected to the rail voltage via bias resistors. Sense units indicate high when the input voltage is above 3.5 V ± 10% and low when the input is below 1.5 V ± 10%.

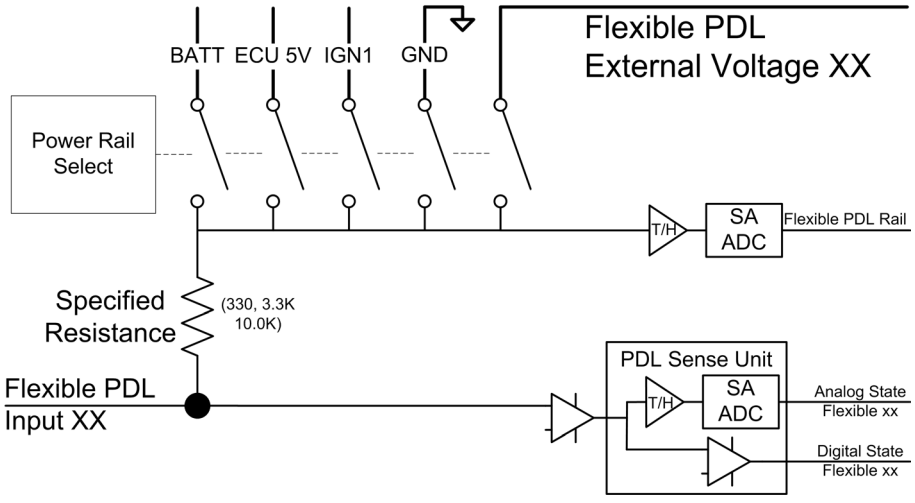


Figure 19: Flexible PDL Input Electrical Diagram

SYNCHRONIZATION

A synchronization pulse that corresponds to the start of a calculation step is generated to enable synchronization between the different modules of the chassis. Because many operations are time related, this pulse is used to latch data (preserve the contents of the previous calculation step) and to reset registers and/or counters for the next time interval.

FIRMWARE UPDATE

TestDrive modules support a robust remote firmware update mechanism. This mechanism is capable to recover from a failure to update FPGA configuration data due to uncontrolled circumstances such as a power failure. In order to recover from such an incident, the FPGA engine includes an FPGA Safe Configuration Data Flash memory device. This memory device holds a bootstrap application code that is common to all Opal-RT modules. These modules are minimal components of any Opal-RT IO controller application allowing a module to be reprogrammed while the model application is in pause.

CONTACT

OPAL-RT Corporate Headquarters

1751 Richardson, Suite 2525
Montréal, Québec, Canada
H3K 1G6
Tel.: 514-935-2323
Toll free: 1-877-935-2323

Technical Services
www.opal-rt.com/support

Note:

While every effort has been made to ensure accuracy in this publication, no responsibility can be accepted for errors or omissions. Data may change, as well as legislation, and you are strongly advised to obtain copies of the most recently issued regulations, standards, and guidelines. This publication is not intended to form the basis of a contract.

11/2013
© OPAL-RT Technologies Inc.

MATLAB, Simulink and Real -Time Workshop are trademarks of The Mathworks, Inc. LabVIEW, MATRIXx, SystemBuild and AutoCode are trademarks of National Instrument s, Inc. QNX i s a trademark of QNX Software Systems Ltd. FireWire is a trademark of Apple Corporation, Inc.

RedHawk i s a tradema r k of Concurrent Corp. All other brand and product name s are trademarks, registered trademarks or service marks of their respective holders. All rights reserved.