OP6224 Pulsed Output Module
User Guide

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PULSED OUTPUT MODULE

INTRODUCTION

The Pulse Output module (POM) is designed to generate bipolar signal with variable frequency and duty cycle. The Pulsed Output module has three types of outputs: Open drain, Analog and Digital.

The board exhibits the following capabilities:

- 24 output channels
- Cable and harness identification
- Module identification and listing
- On site firmware update

ARCHITECTURE OVERVIEW

Figure 20 shows the lock diagram of the Pulsed Output module with the FPGA engine.

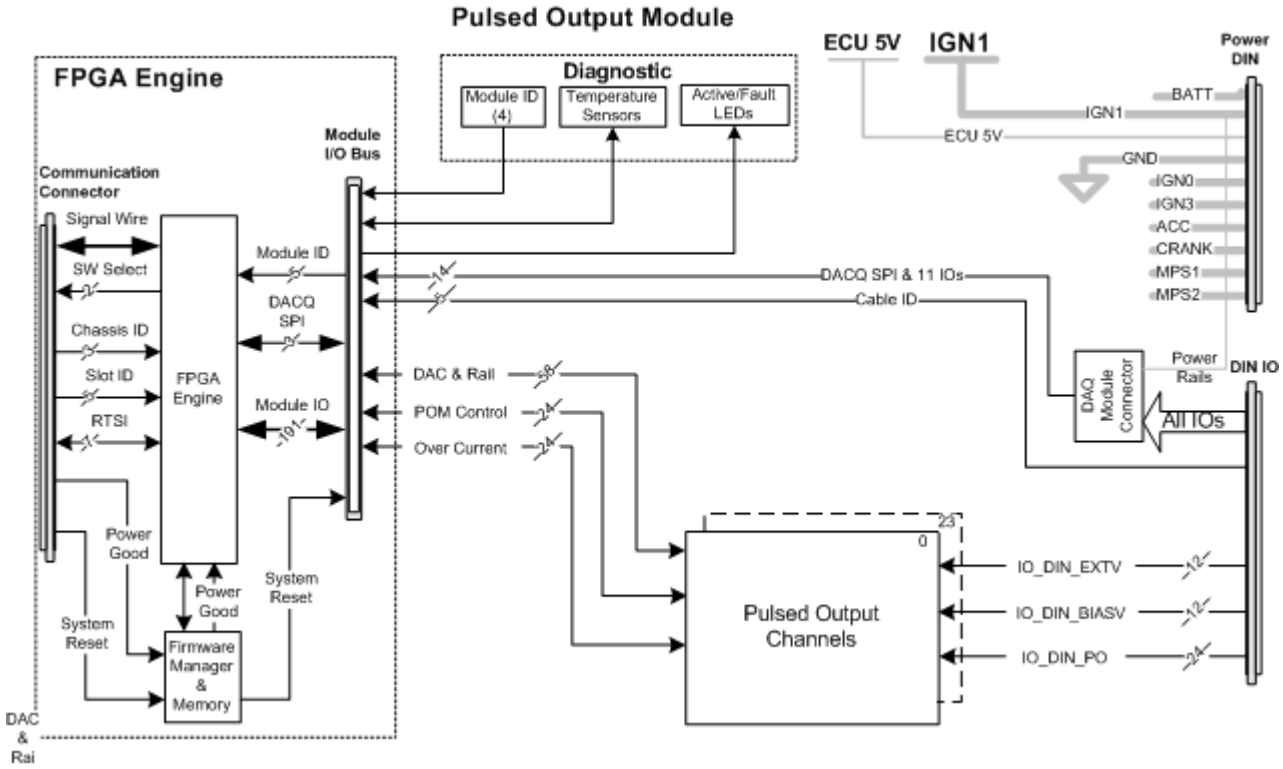


Figure 20: Pulsed Output Module Electronic Board Diagram

Figure 21 shows the block diagram of the Pulsed Output module's embedded firmware. The firmware is mainly composed of the following elements:

- Pulsed Output Unit
- Communication Bus Interface
- Synchronization Unit

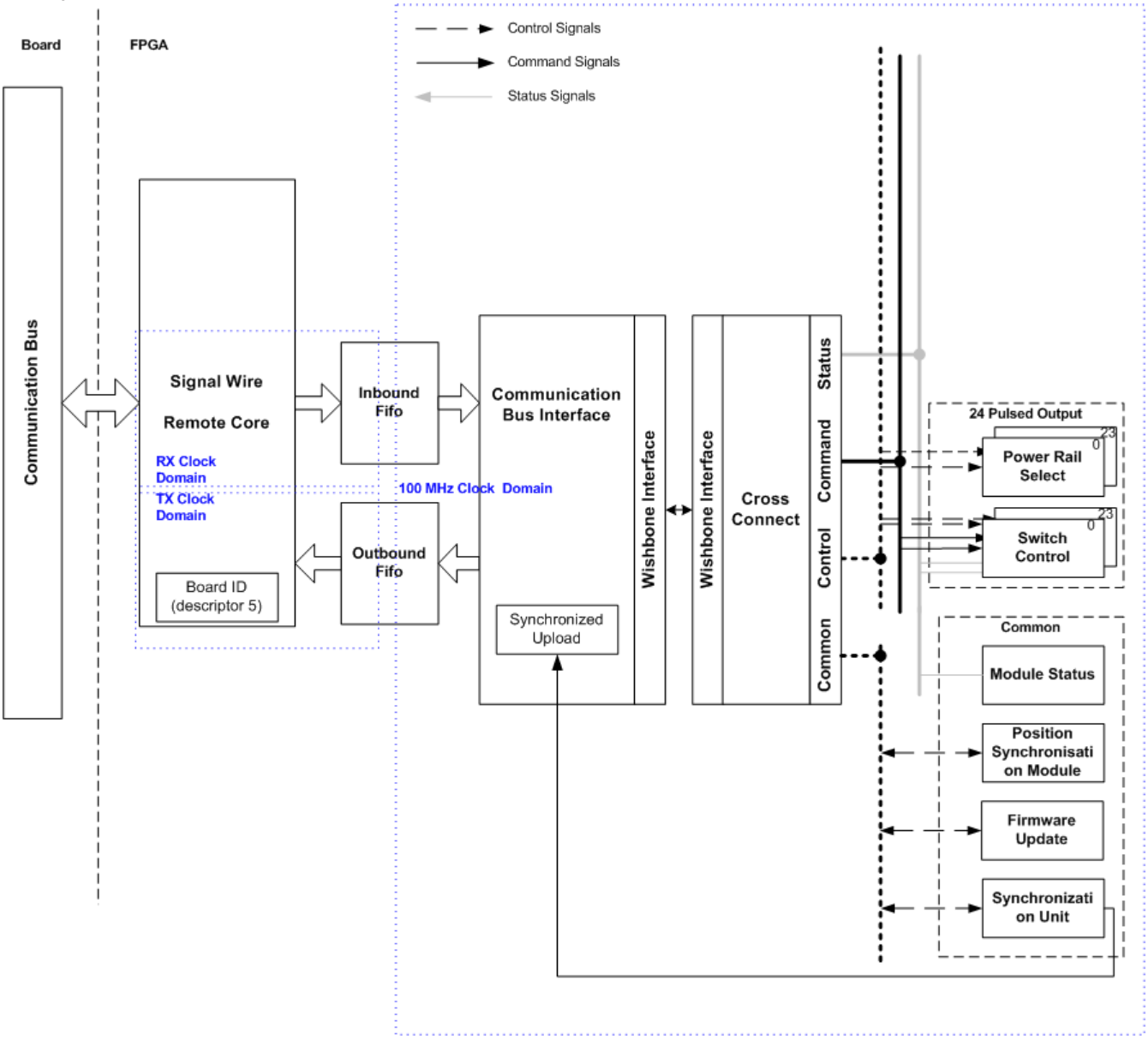


Figure 21: Pulsed Output Module Firmware Diagram

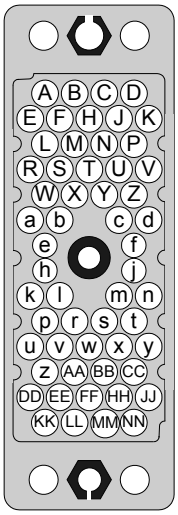
BOARD FEATURES

I/O Connections

The “Pulsed Output Module DIN IO Signal Description” table lists the signals available on the external connector (ELCO-56) and on the system’s backplane (DIN 96/ J7A).

DIN 96/J7A	Signal Name in Pulsed Output Module Schematic (2003/12/06)	Input Line	Output Line
A1	PO1		x
A2	BIASV1	x	
A3	EXTV2	x	
A4	PO6		x
A5	PO7		x
A6	BIASV4	x	
A7	EXTV5	x	
A8	PO12		x
A9	PO13		x
A10	BIASV7	x	
A11	EXTV8	x	
A12	PO18		x
A13	PO19		x
A14	BIASV10	x	
A15	EXTV11	x	
A16	PO24		x
A17	IO_PROTO1	x	x
A18	ID_CBL0	x	
A19	ID_CBL2	x	
B1	PO2		x
B2	PO3		x
B3	BIASV2	x	
B4	EXTV3	x	
B5	PO8		x
B6	PO9		x
B7	BIASV5	x	
B8	EXTV6	x	
B9	PO14		x
B10	PO15		x
B11	BIASV8	x	
B12	EXTV9	x	
B13	PO20		x
B14	PO21		x
B15	BIASV11	x	
B16	EXTV12	x	
B17	IO_PROTO2	x	x
C1	EXTV1	x	
C2	PO4		x
C3	PO5		x
C4	BIASV3	x	
C5	EXTV4	x	
C6	PO10		x
C7	PO11		x
C8	BIASV6	x	
C9	EXTV7	x	
C10	PO16		x
C11	PO17		x
C12	BIASV9	x	
C13	EXTV10	x	

Female
ELCO Connector
56 pins



DIN 96/J7A	Signal Name in Pulsed Output Module Schematic (2003/12/06)	Input Line	Output Line
C14	PO22		x
C15	PO23		x
C16	BIASV12	x	
C17	ID_CBL		x
C18	ID_CBL1	x	
C19	ID_CBL3	x	

Table 10: Pulsed Output Module DIN IO Signal Description

MODULE LEDS

Each module's state is displayed using 3 LEDs:

LED	Indicator	Description
Green	Power	Indicates that the digital power supply for 5 V or 3.3V are within the validity range. This LED is not software controlled
Yellow	Activity	Driven by the FPGA. Indicates that the FPGA has been configured and the communication has been reset by the real-time unit (RTU). This LED shows that the FPGA engine of the module is able to communicate with the RTU The yellow LED indicates error codes when the RED led is ON: • No blink: general error • 2 blinks: the FPGA module is not programmed, you must perform flash update operation. • 3 blinks: the FPGA firmware does not correspond to current module. (e.g. The FPGA is programmed for a Pulse Driven Load Module but is inserted on Switch Module.)
Red	Fault	Driven by the FPGA, the LED indicates that a fault has been detected in the system. These faults are, but not limited to: over tension, over current and software fault. Other software faults are raised under the following conditions: • Invalid configuration, e.g. Enabling several power rails for an output signal • Invalid output driver selection • Invalid model conditions

The FPGA prevents invalid configuration, however, it lets the fault LEDs inform the operator of an abnormal condition. In addition, the error is reported to the model.

SYSTEM IDENTIFICATION

Cable Identification (ID_CBL5-0)

These five input signals are used by the real-time unit to identify which harness connector is attached to the module. Each of these signals is pulled up to 5V through a 100 kΩresistor. When the harness connector is plugged into the simulator it grounds the selected signals to provide the simulator with the cable ID (see Figure 20). For example, if the first and fourth signals (ID 0 and ID3) are shorted to the ground, the simulator returns 22 (10110) for the cable ID.

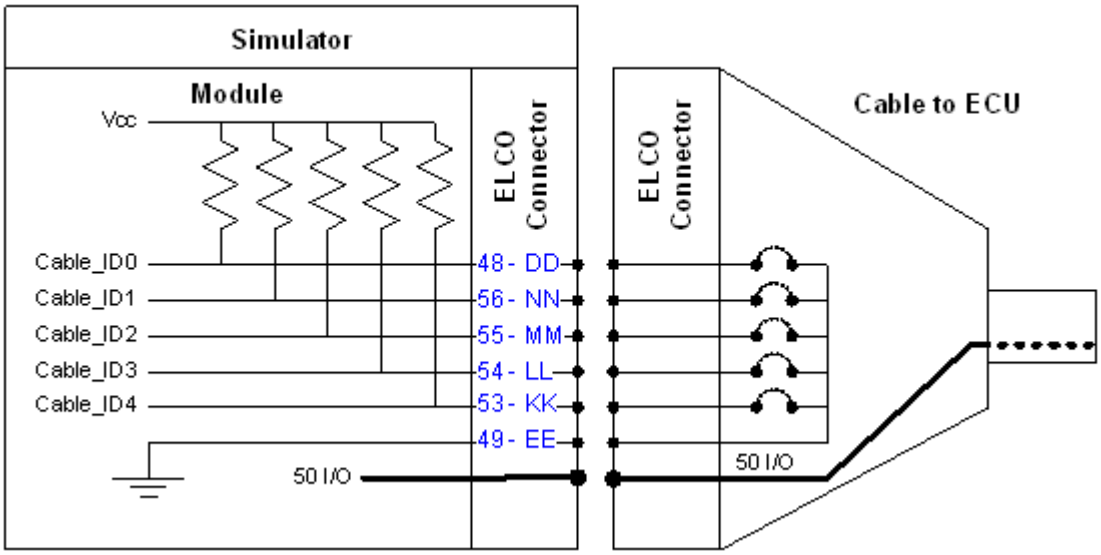


Figure 22: Cable Identification

PULSED OUTPUT

The Pulsed Output Module features 24 channels that can be individually configured for digital or analog mode. In digital mode, you can select a reference voltage then modify frequency and duty cycle. In Analog mode, you can specify amplitude and offset. The signal will be either a bipolar signal (switching for low to high value) or a sine wave. The following table lists the options for each mode.

Output Type	Duty Cycle	Freq.	Adj. Offset	Adj. Ampl.	Reference Voltage		
	[0-100%]	[0-10 KHz]	[± 12V]	[± 12V]	IGN1	ECU 5V	External
Digital	X	X			X	X	X
Analog	X	X	X	X			
Analog Sine	X	X	X	X			

Table 11: Digital and Analog mode summary

Over current and over voltage conditions are monitored for each channel. Faulty channels will be disabled until you acknowledge the error from the user interface.

Figure 23 shows the block diagram of a pulse output channel. An output switch allows you to either the analog or the digital mode.

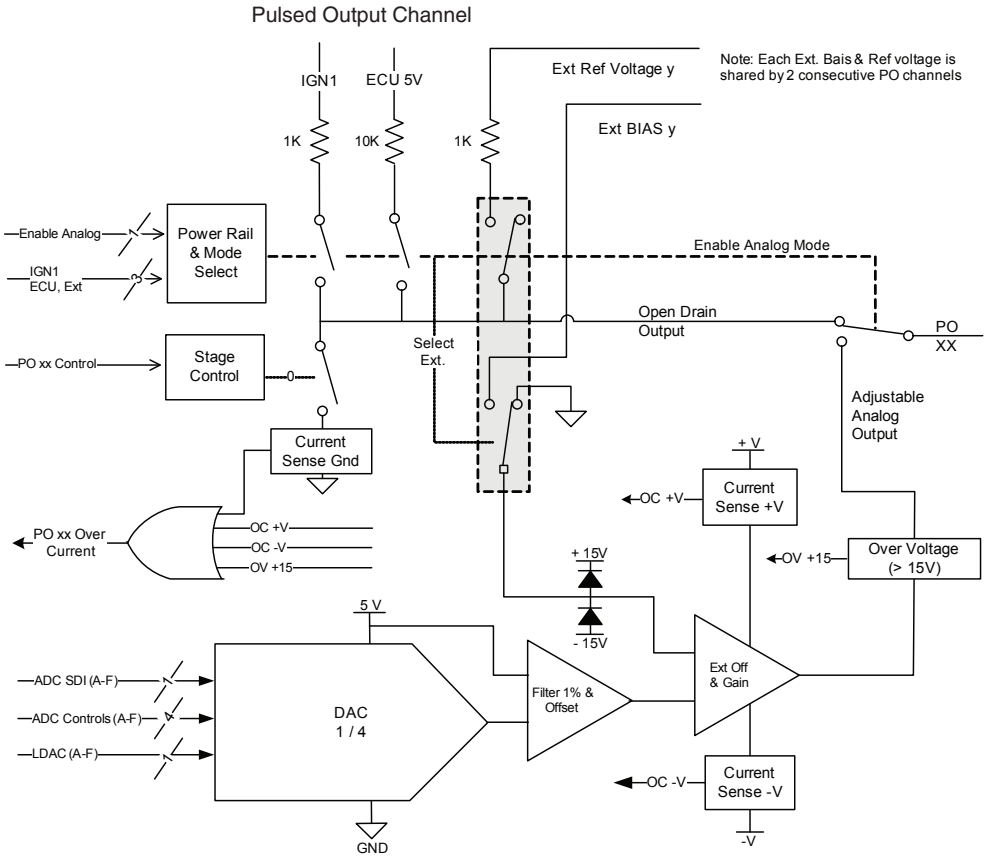


Figure 23: Pulsed Output Channel Diagram

Frequency and Duty cycle precision

The following tables show the Marginal Frequency resolution and the frequency accuracy due to the frequency divider. However, the user should keep in mind that current hardware configuration features a Module Clock frequency of either 100 MHz with 100 ppm (0,01%) or 62,5 MHz with 30 ppm (0,003%). The crystal accuracy factor is not included in the tables below. Tables were calculated with a clock of 62.5 MHz and highlighted numbers in bold indicate characteristics over specification. However, accuracy is met in all cases, at all times.

Frequency (Hz)	Min Resolution (Hz)	Marginal Frequency	Marginal Resolution (Hz)	Actual Freq. Accuracy	Duty Cycle Minimum Resolution
10.000	0.1526	9,996.8	3,199	0.03%	0.03%
5,000	0.1526	4,999.2	0.800	0.02%	0.02%
2,200	0.1526	2,199.8	0.155	0.01%	0.01%
1,000	0.1526	1,000.0	0.032	0.00%	0.00%
500	0.0100	499,992	0.008	0.00%	0.00%
100	0.0100	100,000	0.000	0.00%	0.00%

Table 12: Channel Characteristics in digital mode

Frequency (Hz)	Min Resolution (Hz)	Marginal Frequency	Marginal Resolution (Hz)	Actual Freq. Accuracy	Nb Coefficient
10.000	0.1526	9,949.1	50,939	0.51%	32
5,000	0.1526	4,987.2	12,767	0.26%	32
2,200	0.1526	2,197.5	2,475	0.11%	32
1,000	0.1526	999.5	0.512	0.05%	32
500	0.0100	499,872	0.128	0.03%	32
100	0.0100	99,995	0,.005	0.01%	32

Table 13: Channel Characteristics in analog mode

Digital mode (PO1-24, EXTV1-12)

While using the digital mode, select a rail voltage that is either IGN1, ECU5V or an external voltage. The EXTV1-12 input lines are used when external voltage is selected. Since only 12 lines are available, each line is used for 2 consecutive channels, e.g. EXTV1 is used for PO1 and PO2, EXTV2 is used for PO3 and PO3.

Analog mode (PO1-24, BIASV1-12)

The analog mode is not available in current POM boards.

In analog mode, the output is generated by a Digital to Analog Converter where the output is centered around the offset voltage ±1%. You can select from an external offset voltage (BIASVX) or the one provided internally. The output has a maximum peak to peak voltage of 24 V with a resolution of 0.0234 V ±1% and an accuracy of 1% over the range. The output is able to drive 60 mA.

SYNCHRONIZATION

A synchronization pulse that corresponds to the start of a calculation step is generated to enable synchronization between the different modules of the chassis. Because many operations are time related, this pulse is used to latch data (preserve the contents of the previous calculation step) and to reset registers and/or counters for the next time interval.

FIRMWARE UPDATE

TestDrive modules support a robust remote firmware update mechanism. This mechanism is capable of recovering from a failure to update FPGA configuration data due to uncontrolled circumstances such as a power failure. In order to recover from such an incident, the FPGA engine includes an FPGA Safe Configuration Data Flash memory device. This memory device holds a bootstrap application code that is common to all Opal-RT modules. These modules are minimal components of any Opal-RT IO controller application allowing a module to be reprogrammed while the model application is paused.

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