Reference Pulse Generator Module
User Guide

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REFERENCE PULSE GENERATOR MODULE

INTRODUCTION

The Reference Pulse Generation Module (RPG) serves as the interface for all engine synchronous input and output signals. The RPG generates multiple signal patterns at a selected RPM value and measures spark and injector signal timings.

The board exhibits the following capabilities:

- 13 reference pulse generation channels with a 0.1 degree resolution
- 24 Engine Spark Timing (EST) or Injector inputs
- Knock generation using an arbitrary waveform generator or an external signal
- Cable and harness identification
- Module identification and listing
- On field firmware update

ARCHITECTURE OVERVIEW

Figure 24 shows the block diagram for the Reference Pulse Generation Module with the FPGA engine.

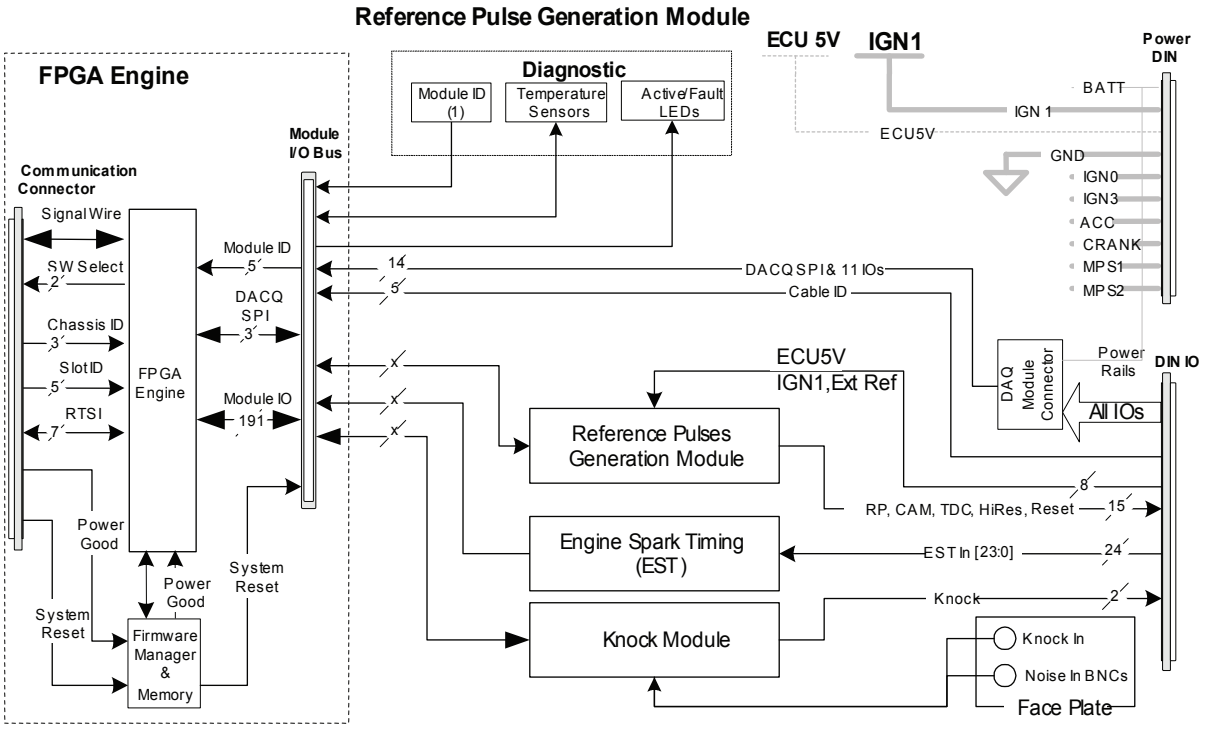


Figure 24: Reference Pulse Generation Module Electronic Board Diagram

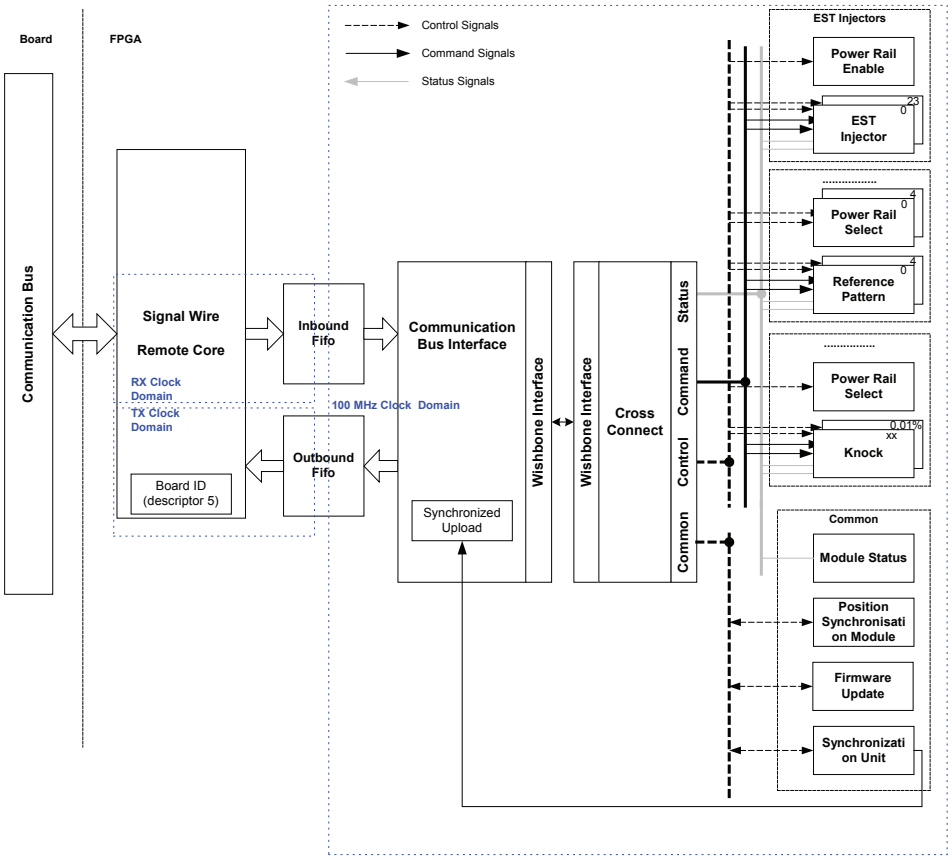


Figure 25: Reference Pulse Generation Module Firmware Diagram

The firware diagram (above) shows the Reference Pulse Generation module's embedded firmware diagram. The firmware is mainly composed of the following elements:

- Communication Bus Interface
- Engine Synchronous Pattern Generation Module featuring Position Encoder and Pattern Generation Modules
- Event Capture module for EST / Injector evaluation
- Knock Control Module
- Power Rail Selection Module
- Synchronization Unit

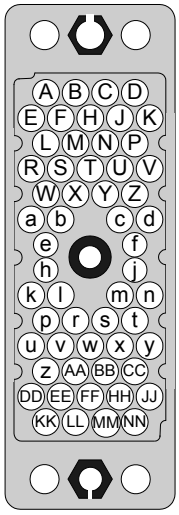
BOARD FEATURES

I/O Connections

Table 14 lists the signals available on the external connector and on the system's backplane.

Elco Eq. # (female)	Elco Pin Name (female)	Signal Name in Resistive Module Schematic	Input Line	Output Line
1	A	INP1	x	
2	B	USR0	x	
3	C	DIN_B1	x	x
4	D	INP0	x	
5	E	USR2	x	
6	F	DIN_B3	x	x
7	H	INP2	x	
8	J	USR1	x	
9	K	DIN_B2	x	x
10	L	INP4	x	
11	M	USR3	x	
12	N	DIN_B4	x	x
13	P	INP3	x	
1	R	USR5	x	
15	S	DIN_B6	x	x
16	T	INP5	x	
17	U	USR4	x	
18	V	DIN_B5	x	x
19	W	INP7	x	
20	X	USR6	x	
21	Y	DIN_B7	x	x
22	Z	INP6	x	
23	a	DIN_B9	x	x
24	b	INP8	x	
25	c	USR7	x	
26	d	DIN_B8	x	x
27	e	INP9	x	
28	f	USR8	x	
29	h	USR9	x	
30	j	DIN_B10	x	x
31	k	INP11	x	
32	l	USR10	x	
33	m	DIN_B11	x	x
34	n	INP10	x	
35	p			
36	r			
37	s	USR11	x	
38	t	DIN_B2	x	x
39	u			
40	v			
41	w			
42	x			
43	y			
44	z			
45	AA			
46	BB			
47	CC			
48	DD	ID_CBL0	x	
49	EE	ID_CBL		x
50	FF			

Female
ELCO Connector
56 pins



Elco Eq. # (female)	Elco Pin Name (female)	Signal Name in Resistive Module Schematic	Input Line	Output Line
51	HH			
52	JJ			
53	KK	ID_CBL4	x	
54	LL	ID_CBL3	x	
55	MM	ID_CBL2	x	
56	NN	ID_CBL1	x	

Table 14: Reference Pulse Generation Module DIN I/O Signal Description

MODULE LEDS

Each module's state is displayed using 3 LEDs:

LED	Indicator	Description
Green	Power	Indicates that the digital power supply for 5 V or 3.3V are within the validity range. This LED is not software controlled
Yellow	Activity	Driven by the FPGA. Indicates that the FPGA has been configured and the communication has been reset by the real-time unit (RTU). This LED shows that the FPGA engine of the module is able to communicate with the RTU The yellow LED indicates error codes when the RED led is ON: • No blink: general error • 2 blinks: the FPGA module is not programmed, you must perform flash update operation. • 3 blinks: the FPGA firmware does not correspond to current module. (e.g. The FPGA is programmed for a Pulse Driven Load Module but is inserted on Switch Module.)
Red	Fault	Driven by the FPGA, the LED indicates that a fault has been detected in the system. These faults are, but not limited to: over tension, over current and software fault. Other software faults are raised under the following conditions: • Invalid configuration, e.g. Enabling several power rails for an output signal • Invalid output driver selection • Invalid model conditions

The FPGA prevents invalid configuration, however, it lets the fault LEDs inform the operator of an abnormal condition. In addition, the error is reported to the model.

SYSTEM IDENTIFICATION

Cable Identification (ID_CBL5-0)

These five input signals are used by the real-time unit to identify which harness connector is attached to the module. Each of these signals is pulled up to 5V through a 100 kΩ resistor. When the harness connector is plugged into the simulator it grounds the selected signals to provide the simulator with the cable ID (see Figure 3). For example, if the first and fourth signals (ID 0 and ID3) are shorted to the ground, the simulator returns 22 (10110) for the cable ID.

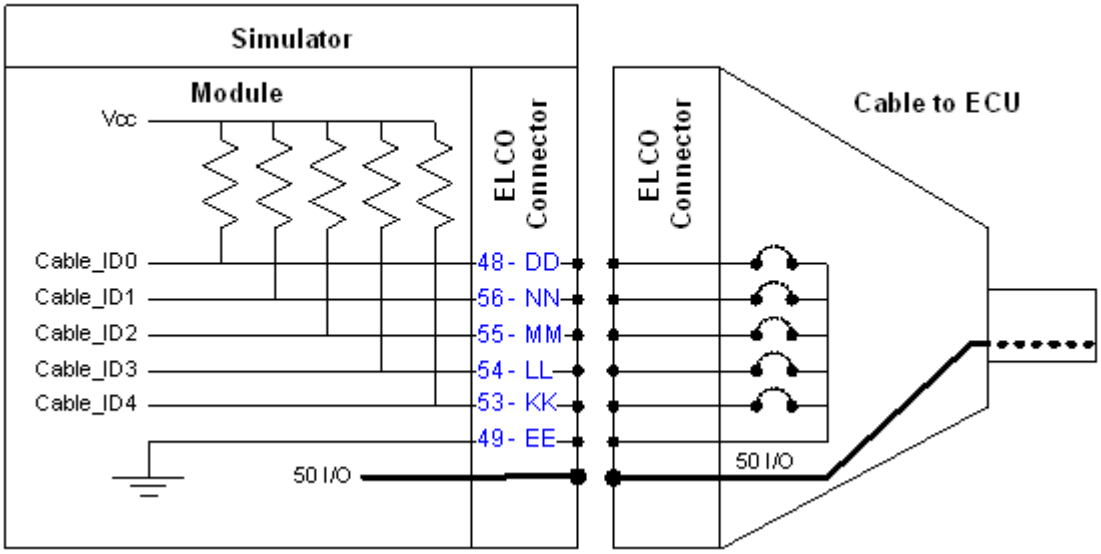


Figure 26: Cable Identification

ENGINE SYNCHRONOUS PATTERN GENERATION

(DIN_RP1-8, DIN_CAM1-4, DIN_TDC)

Engine synchronous pattern generation module allows generation of digital pattern according to specified engine speed. Signal definition is done according to rising and falling edge positions in degrees.

The RPG module has a total of 13 configurable output channels and 2 fixed reference outputs (Ref pulse, RESET). The following table describes possible voltage levels for each output.

Signal	0-5V	0-IGN1	±12V	Open Drain
Ref Pulse	X			
TDC	X			
Reset	X			
Cam Phaser 1-4	X	X	X	X
User Defined RP 1-3	X	X	X	X
User Defined RP 4-8	X			X

Table 15: RPG Output Voltage

OPERATION

At the model level, you first need to supply pattern definitions. This is done using a MAT file with a cell array that contains a dataset of pattern definitions for each channel.

When running the simulation, select the RPM value and the current dataset to be used. The RPG outputs are continuously updated according to the RPM selection. For CAM Phaser 1-4 channels, you can specify a phase offset in degrees for the pattern definition.

RPG outputs are protected for over current using an internal mechanism that will automatically disable faulty channels. You can re-enable a channel by acknowledging the error from the user interface.

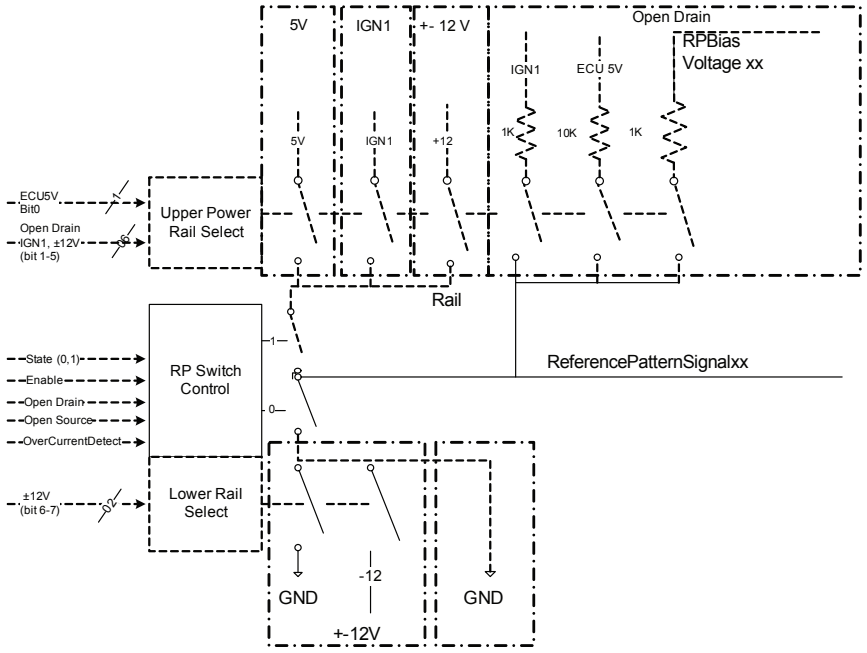


Figure 27: Output stage of the Engine Synchronous Pattern Generation module

EVENT CAPTURE MODULE (DIN_EST0-23)

The event capture module allows you to monitor digital signal to extract pulse rising and falling edge in degrees. In a typical ECU configuration, all sparks and fuel lines will be connected to the Event Capture module.

Operation

The Event Capture module requires an engine synchronous digital signal (0 – 5V or 0 -12V) to be connected to the input. The software extracts all rising and falling transition times and converts them to degrees. For each 720 degrees period, the user interface displays the pulse start and end position in degrees and displays an error code if no or half a pulse is detected. The latching point of pulse positions is configured in the model. By default, each channel is latched with a 60 degrees increment, e.g. INJ0 is latched at 60 degrees, INJ1 is latched at 60 degrees, INJ2 is latched at 120 degrees.)

Knock

The knock feature is not available on the current RPG boards. It will eventually allow you to simulate knock for each cylinder using external signals and arbitrary waveforms.

SYNCHRONIZATION

A synchronization pulse that corresponds to the start of a calculation step is generated to enable synchronization between the different modules of the chassis. Because many operations are time related, this pulse is used to latch data (preserve the contents of the previous calculation step) and to reset registers and/or counters for the next time interval.

FIRMWARE UPDATE

TestDrive modules support a robust remote firmware update mechanism. This mechanism is capable to recover from a failure to update FPGA configuration data due to uncontrolled circumstances such as a power failure. In order to recover from such an incident, the FPGA engine includes an FPGA Safe Configuration Data Flash memory device. This memory device holds a bootstrap application code that is common to all Opal-RT modules. These modules are minimal components of any Opal-RT IO controller application allowing a module to be reprogrammed while the model application is paused.

CONTACT

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