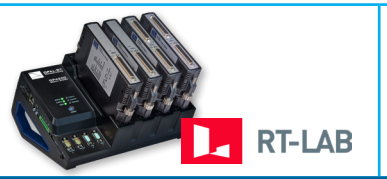
POWER ELECTRONICS

This table provides a comparison and visual summary of core features between several entry-level power electronics testing bundles.

			
	eHS32 Solver | OP4200 **Introductory power electronics HIL simulator**	**eHS64 Solver | OP4510** **Power electronics HIL simulator**	**eHS128 Solver | OP5707** **The most powerful solution on the market**
Part Number	OP42BDL-PE-EHS	OP45BDL-PE-EHS	-
Starting at (Industrial Price)	$8,793 / $9,583	$14,190 / $16,389	CONTACT US
APPLICATIONS			
Single inverter	✔	✔	✔
DC-DC converter	✔	✔	✔
2 x 3 Level back-back (48 switches)	✔	✔	✔
Dual inverter; DC-DC converter; electric motors	-	✔	✔
Hybrid Car drive	-	✔	✔
Dual NPC converter	-	✔	✔
Train drive (4 motors; converter stages; transformers)	-	-	✔
Multiple converters coupled together (scalable UPS system, micro grids, etc.)	-	✔	✔
MMC Converter (up to 512 levels, 2 terminals, 6000 sub-modules)	-	*** 256 levels; two terminals; 3,000 sub-modules	*** 512 levels; two terminals; 6,000 sub-modules
HIGHLIGHTS			
Oversized solver running on FPGA: no need to decouple your models.	Up to 48 coupled switches on 1 FPGA core	Up to 72 coupled switches on 1 FPGA core	Up to 144 coupled switches on 1 FPGA core
Generic and configurable FPGA solver: no need to use VHDL coding or recompile firmware.	✔	✔	✔

*** Optional

Specialized power system solver to optimize real-time performance of Simscape Power Systems (CPU simulation) - Includes the fastest, most accurate solvers for eMEGASIM applications. ARTEMiS solvers and algorithms eliminate artificial delays, while using advanced decoupling techniques for added speed and efficiency.	N/A	***	***
Switching frequency	Up to 200 KHZ	Up to 200 KHZ	Up to 200 KHZ
Test scenarios for automated testing and repeatability	Up to 512	Up to 512	Unlimited (Python, C API)
Control loop minimum delay	1.5 µs	1.5 µs	1.5 µs
Model minimum time step	100 µs (CPU), 125 ns (FPGA)	3 µs (CPU), 125 ns (FPGA)	3 µs (CPU), 125 ns (FPGA)
Co-simulation CPU/FPGA	✔ (1 CPU Core)	✔ (4 CPU Cores)	✔ (Up to 40 CPU Cores)
Machine library PMSM, BLDC, VDQ Model, Induction Machine, Switched Reluctance Machine	N/A	2 machines instances	4 machines instances
SOFTWARE			
RT-LAB | Real-time Simulation Software	✔	✔	✔
Multi editor compatibility: reuse your current models made in SimPowerSystems®, PLECS®, PSIM® or NI MULTISIM®	✔	✔	✔
Supports the Simscape Power Systems & SimPowerSystems® library	N/A	✔	✔
eHS power electronic solver toolbox	eHS32	eHS64	eHS128
ARTEMiS: power electronics/power system solver license	N/A	***	eMEGASIM 1 to 40 Cores Fx
FPGA blockset development system	***	***	***
TECHNICAL SPECIFICATIONS			
Chassis	OP4200	OP4510	OP5700
CPU	Dual-core ARM® Processor Cortex® A9 1 GHz	4 Cores XEON E5 3.5Ghz	XEON E5 3.2Ghz up to 40 Cores
FPGA	Kintex 7 - 7030 - 125K LUT	Kintex 7 – 325T	Virtex 7
Maximum I/O cards per chassis	Up to 4 cards	up to 4 cards	Up to 8 cards
Remote I/O expansion capabilities (HSL)	✔	✔	✔

*** Optional

Analog Output | 16 channels, 16bits, 1 MS/s, +/-16V	***	***	***
Analog Input | 16 channels, 16 bits, 2MS/s, +/-20V	***	***	***
Analog Input | 16 channels, 16 bits, 500 kS/s, +/-20V	***	***	***
Digital Input | 32 channels, 4.5V to 50V, 40 ns	***	***	***
Digital Output | 32 channels, 5V to 30V, 65 ns	***	***	***
Fast optical interface, 1 to 5 Gbits/s	2 ports	4 ports	16 ports
Optional RS422, fiber optic or synchronization modules	-	✔	-
Default RJ45 Ethernet ports	1 port	2 ports	2 ports
Additional RJ45 Ethernet ports (for IEC 61850 and other Ethernet-based protocols)	-	2 ports ***	4 ports ***
RS232, up to 250kbps, full duplex per channel	2	1	1
COMMUNICATIONS PROTOCOLS			
CAN Bus, 1Mbps, half duplex per channel	2 channels ***	4 channels ***	4 channels ***

*** Optional