

RCP TESTING SIMULATOR

The OPAL-RT RCP testing simulator allows models to be run in real-time, without having to code a controller, while also enabling reuse of models on several projects for additional time-savings. OPAL-RT provides a comprehensive software interface, enabling dynamic, real-time tuning and fixing of controllers, significantly reducing test cycle duration. The simple model-based approach enables multiple engineering teams to focus on the most important project aspects, while significantly reducing time spent on reworks. This minimizes the risk of potentially costly mistakes by discovering them earlier in the design process, eliminating negative impacts on costs and scheduling.

OPAL-RT provides a complete range of Rapid Control Prototyping (RCP) solutions to help quickly develop, iterate and test control strategies, while cutting back on development risk, time and cost. Based on MATLAB/Simulink®, RCP real-time simulator lets engineers quickly test and iterate their control strategies on a real-time simulator with real input and output signals, and correct mistakes or make changes in advance—without the need for complex coding and integration.

	RT-LAB OP4200 Small all-purpose RCP system	RT-LAB OP4510 Power electronics RCP system	RCP SYSTEM for fast simulation on CPU & FPGA
Part Number	OP42BDL-RCP-SPS	OP45BDL-RCP-SPS	-
QW Bundles No.	100	110	-
Starting at (INDUSTRIAL/EDUCATIONAL)	\$9,268 / \$7,414	\$15,816 / \$12,652	CALL US
APPLICATION EXAMPLES			
Real-time power electronics/power system core license	3 Cores	1 Core HYPERSIM HX30	UP to 40 Cores
ARTEMiS - power electronics/power system solver license	eMEGASIM 1 Core – Fx75	N/A	eMEGASIM up to 40 Cores
Speed / position control loops validation	Yes	Yes	Yes
Current control loops validation	Optional	Optional	Yes
Model-In-the-Loop, Software-in-the-Loop, Hardware-In-the-Loop simulation	Yes	Yes	Yes
Processor in the Loop simulation	Yes (Zynq®)	-	-
Signal generator	Yes	Yes	Yes
Data acquisition	Yes	Yes	Yes

Protective relay, PMU and SmartGrid IED prototyping	-	Yes	Yes
Electric drive control prototyping	Optional	Optional	Yes
SOFTWARE			
RT-LAB - real-time simulation platform based on MATLAB/Simulink®	included	included	included
FPGA blockset development system (RT-XSG)	Optional	Optional	Optional
TECHNICAL SPECIFICATIONS			
Chassis	OP4200	OP4510	OP5030 or OP5700
CPU	Dual-core ARM® Processor Cortex® A9 1 GHz	4 Cores XEON E5 3.5Ghz	Up to 40 cores XEON E5 or E7
FPGA	Kintex 7 - 125K	Kintex 7 - 325T	Virtex 7 - 485K
Maximum I/O boards per chassis	up to 4	up to 4	8
Remote I/O expansion capabilities (HSL)	Yes	Yes	Yes
Analog output 16 channels, 1 MS/s, 16-bit	1	1	Optional
Analog input 16 channels, 2 MS/s, 16-bit	Optional	Option	Optional
Analog input 16 channels, 500 kS/s, 16-bit	1	1	Optional
Digital input 32 channels, 40 ns high-speed digital I/O	1	1	Optional
Digital output 32 channels, 65 ns high-speed digital I/O	1	1	Optional
Fast optical interface, 1 to 5 Gbits/s	2	4	16
USB 2.0	1	2	2
Optional RS422, fiber optic or synchronization modules	-	Optional	-
Remote I/O expansion capabilities	-	Yes	Yes
Default RJ45 Ethernet ports	2	2	2
Additional RJ45 Ethernet ports (for IEC 61850 and other Ethernet-based protocols)	no	Optional (2)	Optional (4)
RS232, up to 250kbps, full duplex per channel	2	1	-
COMMUNICATION PROTOCOL			
CAN Bus, 1Mbps, half duplex per channel (option)	2 channels (option)	4 channels (option)	-
LIN (v1.3, v2.0)	-	Optional	Optional
Industrial protocols (Modbus, Profibus, EtherCAT)	-	Optional	Optional
Sensing protocols (BiSS-C, Endat, SSI, I2C, SPI)	Optional	Optional	Optional

HIGHLIGHT

Outer control loop frequency (CPU)	< 10 kHz	< 100 kHz	< 100 kHz
Fast control loop frequency (with optional FPGA RT-XSG blockset)	< 1 MHz (option)	< 1 MHz (option)	< 1 MHz
Advanced PWM generation (up to 200 kHz, resolution 5 ns)	Yes	Yes	Yes
RCP Firmware for power electronics - ADC/PWM synchronization	Yes	Yes	
Sensor models (Encoder, Resolver, Hall Effect)	Yes	Yes	Yes
FPGA electric machine library (PMSM, IM, SRM motor models)	n/a	Yes (option)	Yes
Co-simulation CPU/FPGA	Yes (1 CPU Core)	Yes (4 CPU Cores)	Yes (up to CPU 40 cores)
Simulink modeling	Yes	Yes	Yes