AUTOMOTIVE JOURNAL

ni.com

Q2 + 2020

Using Simulation to Improve EV Power Electronics Designs

Electric vehicle (EV) powertrain architectures vary between full battery electric vehicles (BEVs), plug-in hybrid electric vehicles (PHEVs), and various series or parallel hybrid electric vehicles (HEVs), but they all use power electronics to control and convert electrical power in the system.

Power Electronics Testing Presents New Challenges

High Speed

EV power electronics are characterized by fast-switching frequencies in the range of 2 kHz to 20 kHz. The industry wants to speed up these frequencies even more using new designs based on silicon carbide and gallium nitride. Accurately modeling switching behavior requires simulation timesteps at much higher frequencies than this switching speed—often many times faster than can be accomplished in real time with a standard CPU-based simulation system.

Complex Behavior

Electric machines exhibit complex nonlinear behavior such as magnetic saturation and cogging torque. This behavior can be difficult and computationally intensive to model. You can use linear models to test basic embedded controller functionality, but for tuning and optimization, you need to accurately represent the more complex behavior of the system.

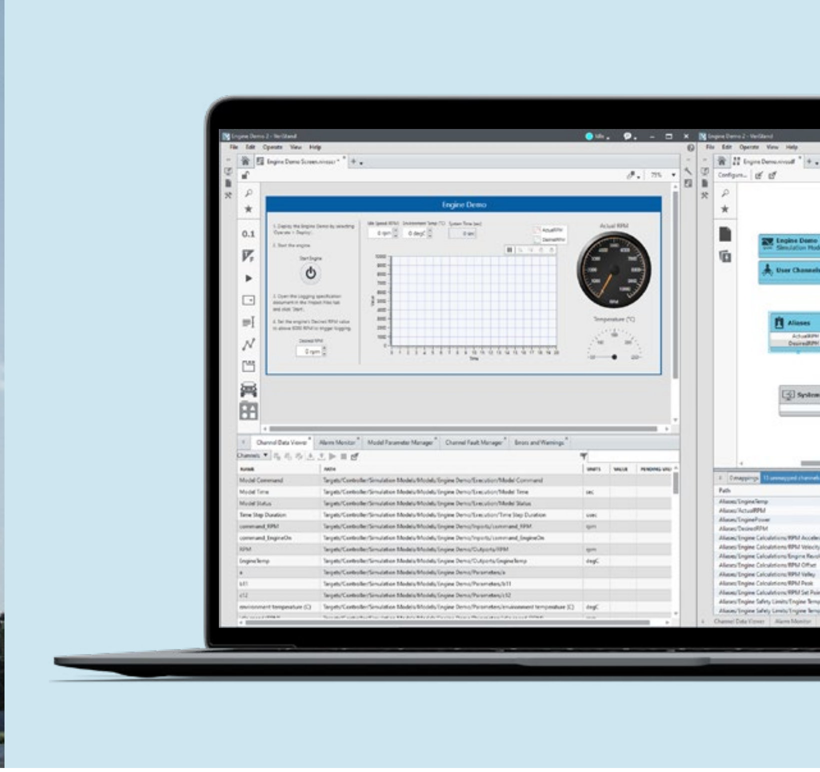
Limitations of CPU-based systems for real-time simulation have made simulation-based methodologies like model in the loop (MIL) and hardware in the loop (HIL) impractical to move earlier in the product development cycle and away from expensive and time-consuming physical test on e-dynos (motor testbenches).

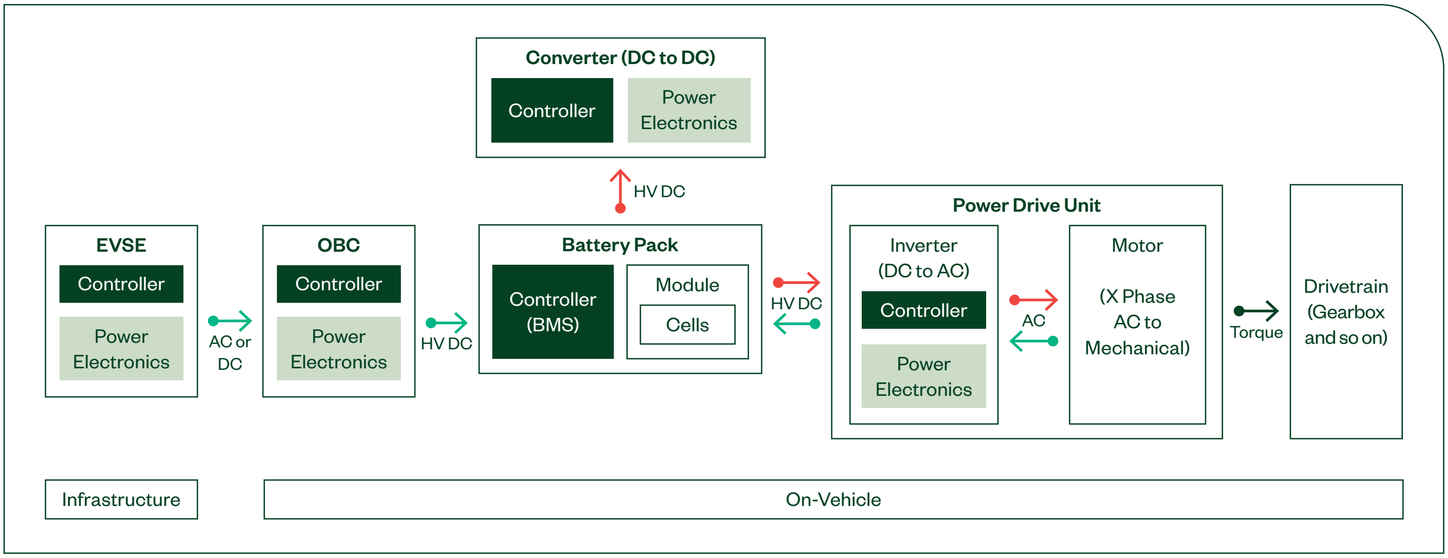
Approach

Use FPGAs for High-Speed Simulation

Achieving adequate simulation speed to enable MIL and HIL testing of EV power electronics means reaching less than 1 s range for simulation periods to execute models that can represent these complex systems with adequate fidelity. Closing the control loop at these speeds requires a paradigm shift away from CPU-based systems to using FPGAs for simulating power electronics and motors.

However, FPGA-based simulation raises new difficulties. Implementing complex power electronics and motor models on FPGAs often requires specialized FPGA-programming knowledge. Also, waiting for lengthy compilations to complete can be a highly iterative process of program, compile, and test.





EV powertrain design is all about managing the flow of power and optimizing power conversion.

Solution

NI Real-Time Test Architecture + OPAL-RT Power Electronics Simulation

NI provides flexible test, measurement, and control with PXI and CompactRIO hardware. Both systems combine a real-time CPU with a user-programmable FPGA and modular I/O. They also run VeriStand software for integrating models with I/O and configuring and running real-time tests.

Both PXI and CompactRIO offer the system architecture you need to realize an FPGA-based simulation approach. With these systems, you can run sophisticated power electronics and motor models at submicrosecond loop rates to provide the simulation fidelity required to return accurate test results and move more testing earlier in the design process.

VeriStand

VeriStand is real-time test software that helps you perform real-time target-to-host communication, data logging, stimulus generation, and alarm detection and response.

VeriStand also transitions quickly from simulation-only testing to HIL testing, which helps you reuse test components such as test profiles, alarms, procedures, and analysis routines. You can remap parameters from models to hardware channels and real-world I/O. This transition saves you time when performing regression testing and helps you automate tests using test executive software such as TestStand.

VeriStand also features an open framework that you can use to create application-specific functionality through add-ons. This provides maximum flexibility in your test system.

OPAL-RT

Power Electronics Add-On for VeriStand

NI collaborates with NI Partner OPAL-RT to provide its FPGA-based Power Electronics Add-On for VeriStand. Integrated directly with VeriStand and extensible with a LabVIEW software development kit, the add-on is a powerful FPGA-based power electronics and motor simulation tool that includes the following:

- OPAL-RT's electric Hardware Solver (eHS), which is a powerful floating-point solver you can use to simulate an electric circuit on an FPGA without having to write the mathematical equations. Import models from various popular schematic editors for power electronics simulation such as MathWorks Simscape™ Electrical™ Specialized Power Systems Library, Plexim PLECS, Powersim PSIM, and NI Multisim. You can choose the eHSx64 or eHSx128 to match the complexity and size of your power electronics topology (the number of states, switches, and measurement and control signals in your system).
- Machine model solvers including permanent magnet synchronous machine and induction machine configurations as well as position feedback devices like resolvers and encoders.
- Multiple supported 2D and 3D solvers that enable tabular import of machine characteristics from finite element analysis or experimental data.
- Signal generation engines, such as sine wave, pulse width modulation (PWM), and sinusoidal PWM, built directly into the FPGA design to generate control signals for open- and/or closed-loop testing.
- The ability to change parameters during simulation using customized test scenarios and parameter sets to generate faults and automate testing without reloading or recompiling your model.

Results

With the NI and OPAL-RT solution, you can implement submicrosecond model-based simulations of power electronics and motors on an FPGA for high-accuracy MIL design studies. You can connect these models to high-performance FPGA-enabled I/O to implement high-performance HIL test systems.

With modular hardware and open software, you can tailor your test system to each specific application while maintaining a consistent test architecture between systems and over time as you upgrade to address changing test requirements. This solution helps you shift test earlier in the design process so you can find problems more quickly, optimize performance sooner, and achieve greater test coverage while shortening test times and reducing total cost of test.

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